AD 295 162

ASD-TDR-62-1033

AUTOMATIC REMOTE TUNING SYSTEM
for
GROUND - AIR UHF COMMUNICATIONS

Technical Documentary Report ASD-TDR-62-1033

21 January 1963

Prepared for

ELECTROMAGNETIC WARFARE AND COMMUNICATIONS LABORATORY
Aeronautical Systems Division
Air Force Systems Command
Wright-Patterson Air Force Base, Ohio

Project No. 4335, Task No. 4335D8

Prepared under Contract No. AF33(616) 7311 by

THE BENDIX CORPORATION
Bendix Radio Division
Baltimore 4, Maryland

NOTICES

When Government drawings, specifications, or other data are used for any purpose other than in connection with a definitely related Government procurement operation, the United States Government thereby incurs no responsibility nor any obligation whatsoever; and the fact that the Government may have formulated, furnished, or in any way supplied the said drawings, specifications, or other data, is not to be regarded by implication or otherwise as in any manner licensing the holder or any other person or corporation, or conveying any rights or permission to manufacture, use, or sell any patented invention that may in any way be related thereto.

Qualified requesters may obtain copies of this report from the Armed Services Technical Information Agency, (ASTIA), Arlington Hall Station, Arlington 12, Virginia.

Copies of this report should not be returned to the Aeronautical Systems Division unless return is required by security considerations, contractual obligations, or notice on a specific document.

ASTIA release to OTS not authorized.

FOREWORD

This final report by the Radio Division of the Bendix Corporation covers the work done to fulfill the requirements of Exhibit A dated 15 May 1959, and amendment number 1, dated 17 February 1961, of task number 433514.

Appropriation for this development program was made through the Deputy for Technology, Directorate of Avionics, Electromagnetic Warfare and Communications Laboratory, of the Aeronautical Systems Division of the Air Force System Command by contract AF33(616)7311. The program was begun in May 1960 and terminated 23 April 1962.

The contract was divided into two tasks:

a. Study, design and develop an Automatic Remote Tuning System for Ground-Air UHF communications

b. Study, design and develop a completely solid state tuning device for operation in the UHF band.

Mr. H. J. Schmidt ASRNCS-3 is the Air Force project engineer assigned to the contract at the Air Force Aeronautical Systems Division. Mr. W. D. Philips was the Bendix project engineer assigned to this contract. This report was prepared by Mr. W. D. Philips and is approved by Mr. W. R. Richardson, Chief Engineer of Communication and Navigation Advanced Department of the Bendix Radio Division.

Recognition is given here to the following engineers who contributed material for this final report:

Mr. D. E. Welch

Mr. D. J. Settlemire

Mr. W. R. Trussell

Mr. R. R. Wilkie

Mr. G. H. Woppman

Mr. W. H. Stotz

Contractor's Report No. 471-938-490

ABSTRACT

The objective of this contract was to develop two control systems. One, an Automatic Remote Tuning System for ground-air UHF communications, and the other system, a UHF Solid State Tuning Device utilizing all solid state components.

The Automatic Remote Tuning System is a system which tunes an airborne AN/ARC-34 UHF communications transceiver from the ground through the selective calling AN/URA-22 (Discom) system. The equipment is completely of solid state construction.

The UHF Solid State Tuning Device is a 1750 channel UHF receiver which is tuned by use of varactor diodes. There are no moving parts in the receiver. The frequency synthesizer is also unique in that all frequencies are obtained from a single crystal oscillator and are phase locked to this stable source.

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

LIST OF ILLUSTRATIONS (Continued)

LIST OF ILLUSTRATIONS (Continued)

1. INTRODUCTION

This is the final report on the Automatic Remote Tuner project conducted by the Bendix Radio Division of the Bendix Corporation for the United States Air Force under contract AF33(616)7311. This report is submitted in accordance with Item IV of the contract and was prepared in accordance with AFSC manual Nr. 5-1, "Preparation of ARDC Technical Documentary Reports."

For readability, a straight-line history of the program is presented in six main sections with supporting details supplied in three appendices.

Section 2 gives a brief outline of the history of the contract and an outline of the change of the contract study program. Section 3 describes briefly the Automatic Remote Tuning section of the contract. Section 4 describes the UHF Solid State Tuning Device. Section 5 contains the description and theory of operation of the ancillary equipment. (The ancillary equipment is that category of equipment which contains subassemblies, such as power supplies, IF amplifiers, etc.) Section 6 presents conclusions of the program and makes recommendations.

The three appendices describe in more detail the numerous investigations undertaken, the results of tests and the tuning or test procedures.

NOVEMBER 1962

Manuscript released by the author for publication as an ASD Technical Documentary Report.

2. CONTRACT HISTORY

Work on the Automatic Remote Tuning System contract was begun in May of 1960, and a working model of this unit was demonstrated to the personnel of the Electromagnetic Warfare and Communications Laboratory ASD during March of 1961. The Automatic Remote Tuning System is a device which is capable of tuning an airborne AN/ARC-34 UHF Communication set automatically from the ground.

The task of the contract was augmented by an amendment to the original exhibit and work was begun on the new task in September of 1961. The work program outlined by Amendment #1 to Exhibit A was to study devices and techniques which eliminate mechanical tuning mechanism, and develop a digital counter type frequency synthesizer. The end result of the program was to develop an UHF communication set which is capable of rapid tuning (one second maximum between channel changes), with no moving parts.

The contract was cancelled 23 April 1962 in order to regroup Air Force funds. At the time of cancellation the project was approaching completion. Permission to complete the system hardware was given to Bendix by the Air Force, providing all funds contracted after 23 April 1962 and expended in completing the hardware would be provided by Bendix, and the final report of the contract would cover the completed task. In conformance it was agreed that Bendix could retain the amendment #1 hardware for demonstration to government and private agencies after demonstration to ASD personnel.

This report therefore covers the contract task to completion.

3. AUTOMATIC REMOTE TUNING SYSTEM

This Section of the report summarizes briefly the system designed in the first phase of the contract. The system has previously been reported in detail by WADD Technical Note 61-40, released April 1961. Copies of this technical note can be obtained from the Armed Services Technical Information Agency (ASTIA) Arlington Hall Station, Arlington 12, Virginia.

The Automatic Remote Tuning System is an all solid state device which is capable of tuning an airborne RT-263/ARC-34 communications set from the ground. This is accomplished by utilizing the equipment shown in Figures 1 and 2 in conjunction with a Selective Calling device known as an AN/URA-22 (Discom) system. The airborne hardware (not including the AN/URA-22 or AN/ARC-34) is shown in Figure 1, and the ground station Automatic Remote Tuner equipment with its top cover removed is shown in Figure 2.

The following is a list of system requirements which were used as a guide during the study phase of the contract and later incorporated into the hardware:

a. The system shall be capable of tuning a communications set in a remote vehicle from one frequency to another without the pilots aid.

b. A selective calling device, the AN/URA-22 (Discom), shall be included in the system to allow remote tuning of a selected vehicle.

c. The system will consist of two primary equipments: (a) a ground station which originates and transmits the tuning message and (b) an airborne station which receives the message and tunes the associated equipment accordingly.

d. A subscriber at a point remote to the ground station shall be capable of tuning the vehicle via the ground station.

e. The ground station will normally know the frequency to which a particular aircraft is tuned.

f. The guard channel will be used to contact an aircraft if a priority or urgent communication requirement is present and the aircraft frequency is unknown.

g. All priority tuning messages will be transmitted on the guard channel.

h. Subscriber tuning instructions will provide for tuning the airborne radio set to a communications channel designated for each ground station.

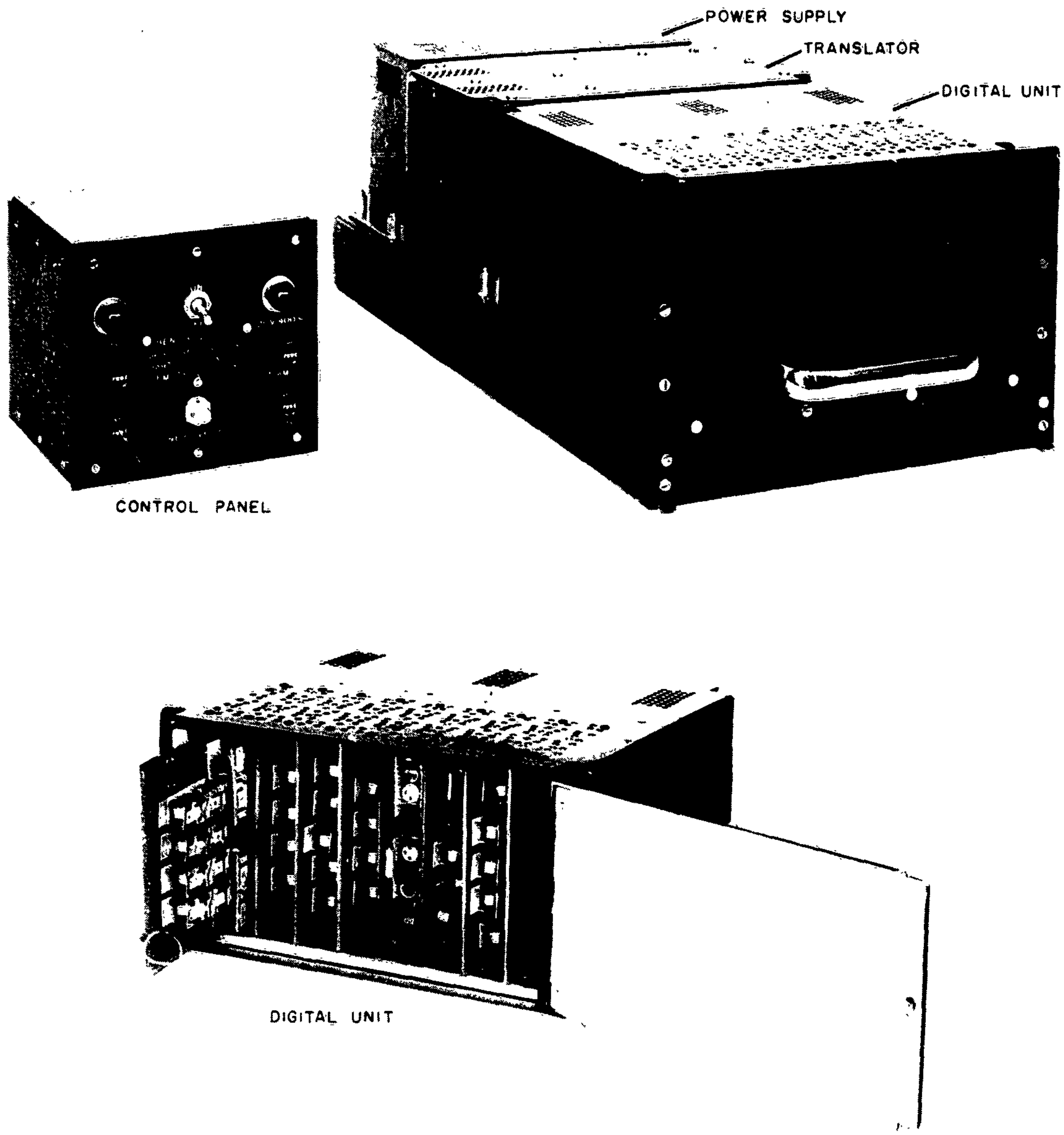


Figure 1. Automatic Remote Tuner Airborne Equipment

Figure 2. Automatic Remote Tuner Ground Station Equipment

i. The only tuning override required by the vehicle operator is the ability to reject an automatic tuning message and return the radio to its previous setting. This override may be accomplished by momentarily switching to the guard position, thereby disabling the remote tuning function.

Operation:

The operation of the automatic remote tuning system which meets these system requirements is described below. The system contains two separate sections: a ground based unit and an airborne unit, both of which work in conjunction with an AN/URA-22 Discom, a selective calling equipment. Tuning and aircraft identification messages are originated at the ground station and transmitted over the proper communications link to the specified aircraft which receives the tuning message and retunes its radio set accordingly.

Ground Station:

Figure 3 is a block diagram of the ground station. The blocks enclosed in dotted lines are the actual automatic remote tuning system. The radio sets and the Discom unit are considered auxiliary equipment. Reference to Figures 4 and 5 will aid the reader in following the procedure used in transmitting a tuning command to an aircraft in flight.

Initially, the operator selects the new frequency to which the aircraft radio will be tuned on the frequency insert unit (keyboard) and observes this input information on the display unit. The transmitter mode is then selected. For a routine transmission this would be the tower frequency; for a priority situation it would be the guard frequency. The operator inserts into Discom the call letters corresponding to one of three situations: (1) individual call, (2) group call, and (3) general call. The mode of the Discom is set to ST. The S refers to silence (no acknowledgement required); the T means that tuning information will be sent.

Next, the actuate button on the ground control panel is depressed, causing a pulse to be sent to the mode selector which keys the desired ground transmitter and connects the modulator input to the Discom output. The same pulse that the mode selector receives also goes to the Discom which, upon receiving the pulse, sends the preamble to the selected transmitter via the mode selector.

At this point the shift register has stored the inserted tuning information, and upon receiving an end-of-preamble pulse from Discom, it sends the tuning information through the mode selector to the proper transmitter. The transmitter is selected when the mode selector receives the end-of-preamble pulse from the Discom. At the end of the tuning information from the shift register, a pulse is produced that (1) causes the mode selector to select the command channel transmitter, thereby connecting the modulator input of this

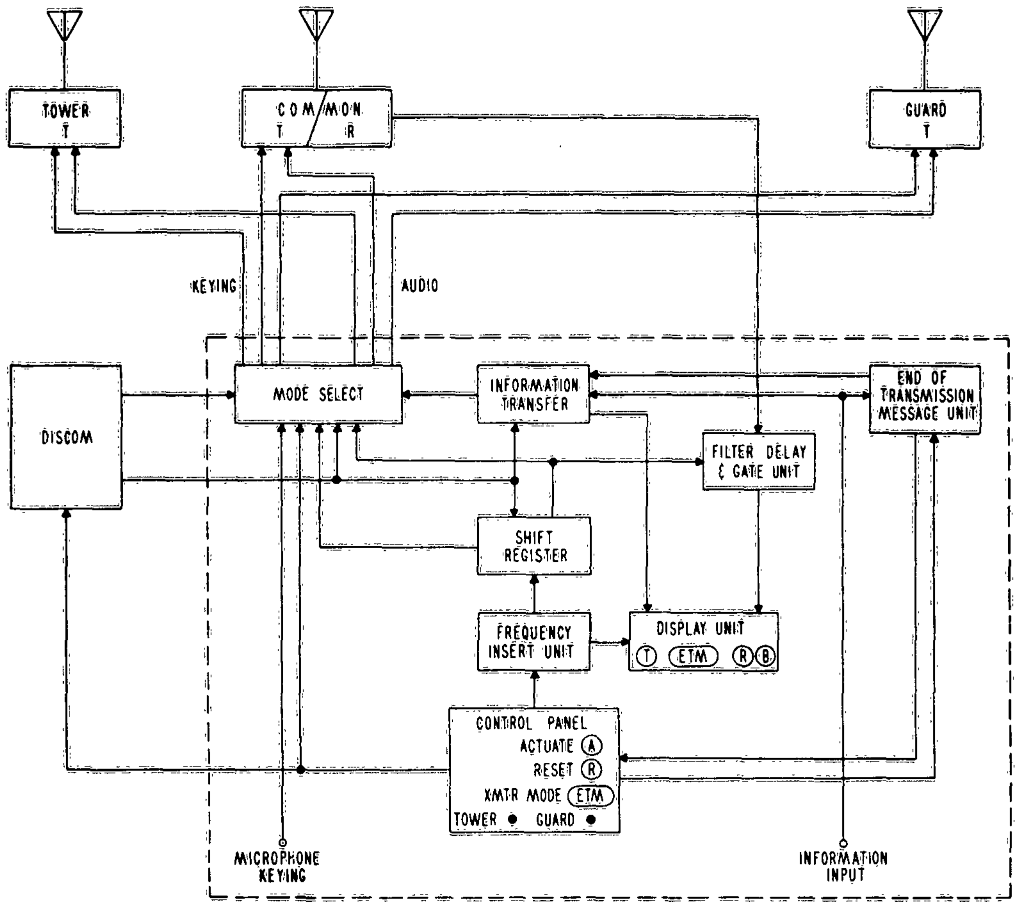


Figure 3. Ground Station System Block Diagram

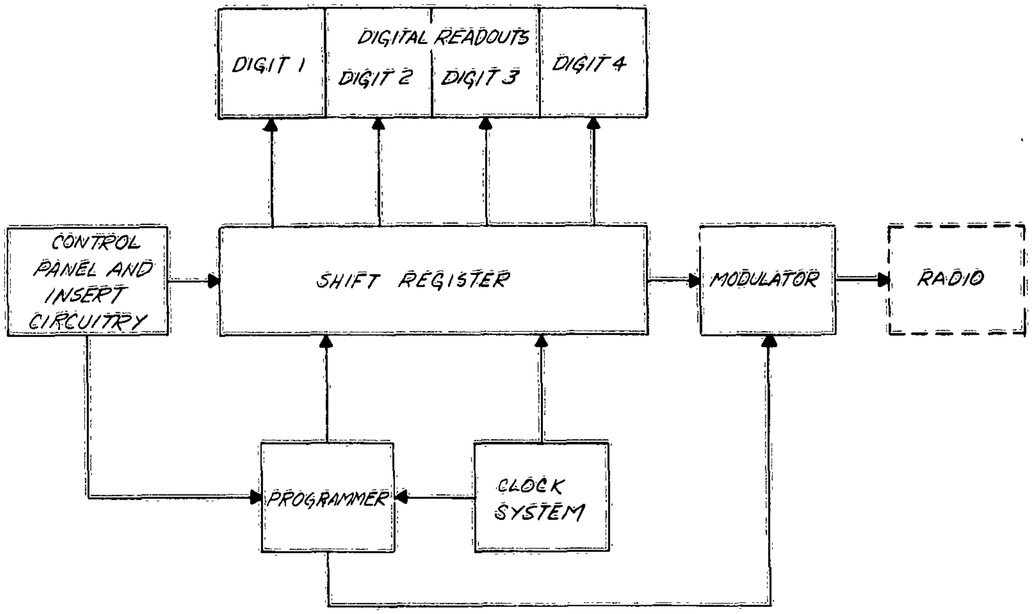


Figure 4. Ground Station Controller Block Diagram

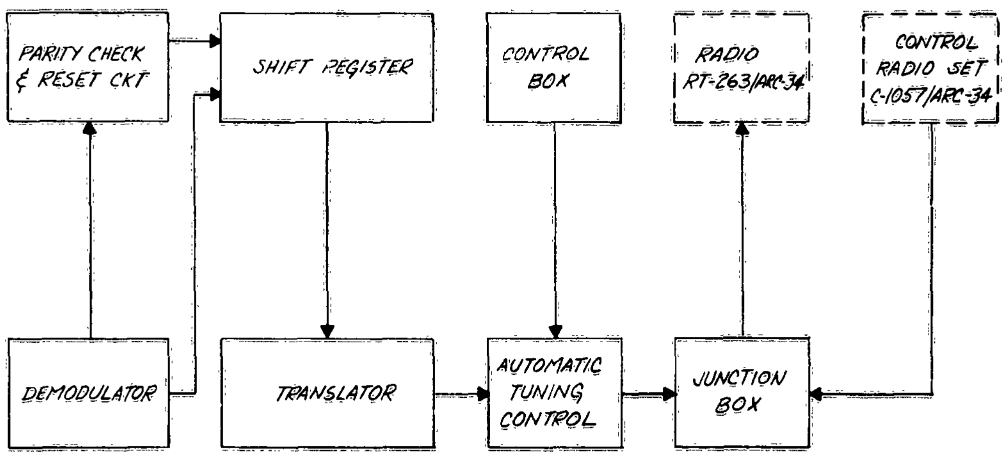


Figure 5. Airborne Controller Block Diagram

Airborne Station:

The airborne equipment (see Figure 6) allows a ground operator to automatically tune the aircraft's radio set while the aircraft is in flight. It will be used in conjunction with Control Monitor Group AN/URA-22(XA-1) (Discom), which enables the ground operator to contact one or a group of aircraft radios. After the intelligence transmission to the aircraft has been completed, the aircraft's tuner equipment automatically tunes the radio to its setting prior to the ground station's call.

Assume that the aircraft's radio is tuned to the tower frequency and that the tuning message from the ground tuning station is transmitted on that frequency. The received Discom preamble from the grount station is recognized by the Discom in the aircraft, providing that it has the correct address, and Discom accepts the information from the ground. In the case of tuning information, the mode of Discom preamble would be ST, the S indicating silence (no acknowledgement required) and the T indicating tuning information. The Discom therefore causes the receiver output to be connected to the remote tuner, which is prepared to accept the incoming tuning information. After the tuning information is received and stored (required time is 35 milliseconds), it produces a pulse which (1) clears Discom, (2) causes the remote tuner to take command of the radio set control box, providing the proper information to tune the set to the frequency commanded by the ground tuning station (GTS), (3) triggers a tone burst generator to cause a "beep" in the pilot's headset, indicating that the radio set is being tuned, (4) operates a light on the pilot's radio control panel, further indicating that the radio set is being tuned, and (5) triggers a delay circuit. The delay circuit allows the radio set sufficient time to tune to the new frequency (about four seconds in the ARC-34), after which it produces a pulse that causes a tone burst from the acknowledge burst generator to be transmitted on the new frequency.

The aircraft now receives another Discom preamble on the new frequency and the mode of the preamble indicates what type of message will follow. The intelligence transmission is then handled in a routine manner. At the end of the intelligence transmission, the ground tuning station transmits an end-of-transmission message. This message is recognized by the remote tuner, which remained connected to the receiver output, and the remote tuner switches control of the radio set back to the pilot's control box. The aircraft's radio set, therefore, tunes to the frequency to which the pilot's control box is set. At the time this occurs, a tone is sounded in the pilot's headset, and the indicator light on the control panel goes out. Both of these are indications to the pilot that he has regained control of the radio set.

transmitter to the output of Discom, and (2) causes a delay and gate unit to operate. The delay is approximately 4 to 6 seconds (aircraft tuning time), and at the end of the delay, a gate is opened to accept the acknowledgement pulse from the aircraft. The generation of this pulse is described in the following airborne equipment section.

After the preamble and tuning information has been transmitted on the selected frequency (tower or guard), the ground tuning station waits for an acknowledgement in the form of a tone burst (pulse) for a short interval of time. If it arrives at the correct time, it is passed through a filter, delay, and lights the ready light on the ground display unit. If the pulse does not arrive at the correct time, the busy light goes on and indicates to the operator that the aircraft is not tuned to the selected frequency.

Assuming an aircraft has sent an acknowledgement and the ready light is lit, the operator can now transmit the intelligence. He again engages the actuate button, and the common transmitter is keyed and the Discom preamble is transmitted as before. The end-of-preamble pulse now has no effect on the shift register, but triggers the information transfer to allow the intelligence to be transmitted. The end-of-preamble pulse also selects the proper setting of the mode select to connect the output of the information transfer to the common transmitter modulation input. As soon as the information transfer has been cleared for an intelligence transmission, a transmit light is lit on the control panel to indicate to the operator that transmission can begin. The trigger pulse that causes the light to be lit may also be used to start canned messages, etc. In the case of voice transmission the light is a visual indication to begin speaking. When voice transmission is employed it is realized that the transmitter is already keyed. When this button is depressed, it causes a change in the mode select so that when the button is released the transmitter is not keyed. Therefore, keying is accomplished only when the microphone button is depressed. When the end-of-transmission message (ETM) button is engaged at the end of the voice transmission, the mode select is reverted to the condition prior to depressing the push-to-talk button on the microphone.

When the intelligence transmission has been completed, the end-of-transmission message is transmitted either automatically or manually. In the case of prearranged and canned messages, it can be sent automatically by placing the ETM switch on the control panel A, or automatic. For voice transmissions, however, it must be initiated manually. When the ETM switch is on M, or manual, the transmission message must be sent by engaging the ETM button on the control panel.

When the ETM unit has sent the message, it provides a reset pulse which is fed to the control panel to clear the shift register which has stored the tuning information, to cause the lights on the display unit to go out, to reset the mode select to the tower radio set, and to reset the information transfer channel.

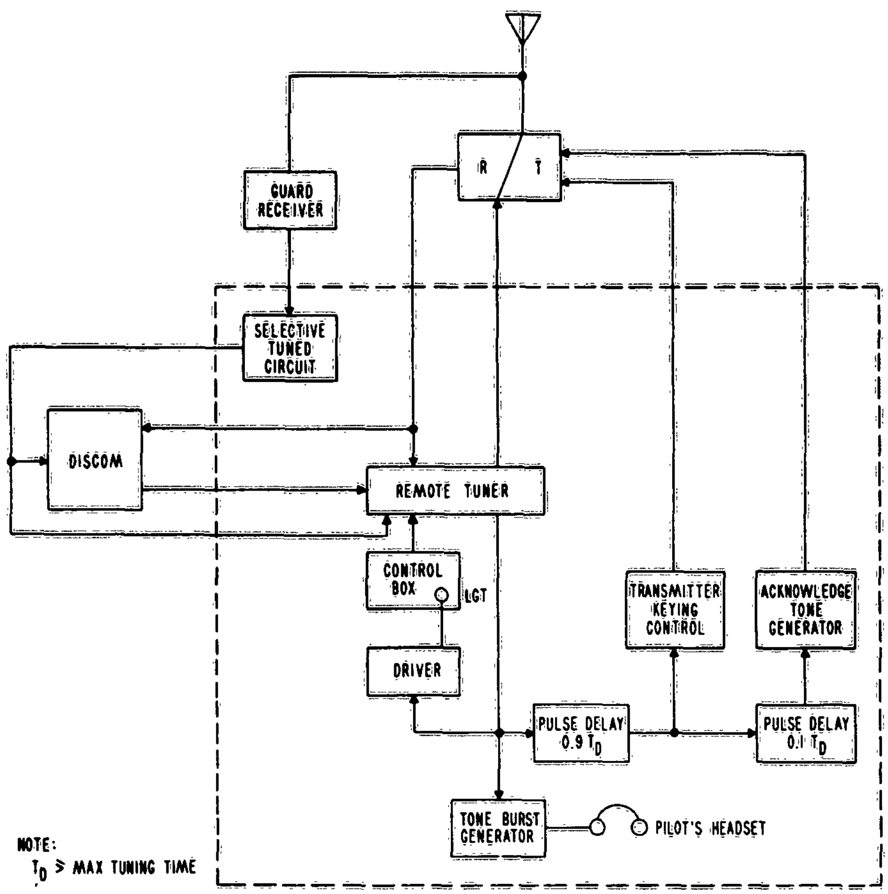


Figure 6. Airborne Unit System Block Diagram

4. SOLID STATE TUNING DEVICE

The Solid State Tuning Device is shown in Figures 7 and 8 and a block diagram of the system is shown in Figure 9.

Those units that are tuned by the frequency selector (Front End, Harmonic Generator, VFO, and Digital Synthesizer) are described in detail in paragraphs 4.1, 4.2, 4.3 and 4.4, respectively.

Those units that are considered as ancillary equipment (not part of the study program) such as the IF Amplifier, Second Mixer, Reference Generator, Power Supply, and Frequency Control Panel are described in detail in paragraphs 5.1, 5.2, 5.3, 5.4 and 5.5, respectively.

The solid state tuning device is an electronically tuned UHF communications receiver. The tuning is accomplished by electronic means, thereby eliminating some of the undesirable features of mechanical tuning such as its susceptability to shock and vibration, its slowness of tuning, and its high current switching requirements. In contrast, the solid state tuning device can be made nearly insensitive to mechanical disturbances, it tunes instantaneously to any channel, and no high current devices are required to accomplish the tuning.

The frequency stability of the receiver is determined by the accuracy of its reference generator. Crystal oscillators with accuracies in the order of one part in 10^6 are easily obtained with little or no complexities. If an oscillator of this accuracy is used in conjunction with crystal filters in the IF amplifiers, an AM voice channel spacing of 25 Kc is entirely feasible in the UHF band.

This stability is maintained by a phase locked system comprised of a variable frequency oscillator and a digital synthesizer. The synthesizer contributes no appreciable frequency instabilities to the system, thereby allowing the reference generator to determine the system stability.

The only problem area concerning the digital synthesizer and phase locked oscillator used in this system is frequency modulation or phase jitter in the oscillator. These undesirable effects can be minimized by careful filtering of the preset tuning voltage from the frequency selector to the VFO and elimination of AC components on the analog control lines from the digital synthesizer to the VFO. (Phase locked loop)

The system developed on this contract is capable of maintaining a good noise figure (approximately 8 db) through 85 percent of the UHF band. The noise figure deteriorates at the low frequency end of the band. A good sensitivity (5 uv for 6 db $\frac{S+N}{N}$) can be maintained down to 250 Mc. At 240 Mc the sensitivity has dropped to approximately 10 uv and at 225 Mc the sensitivity is approximately 30 uv. This loss in sensitivity is easily explained in that the Q of the varactors used to tune the front end has deteriorated until the gain of the front end is down

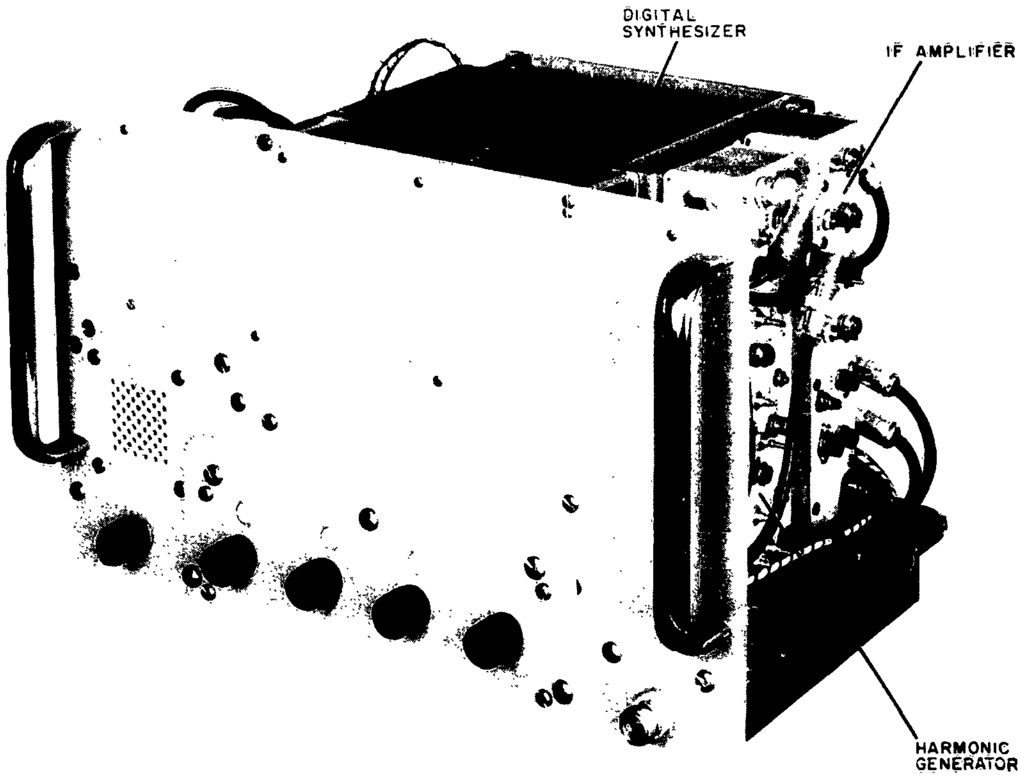


Figure 7. Solid State Tuning Device (Front View)

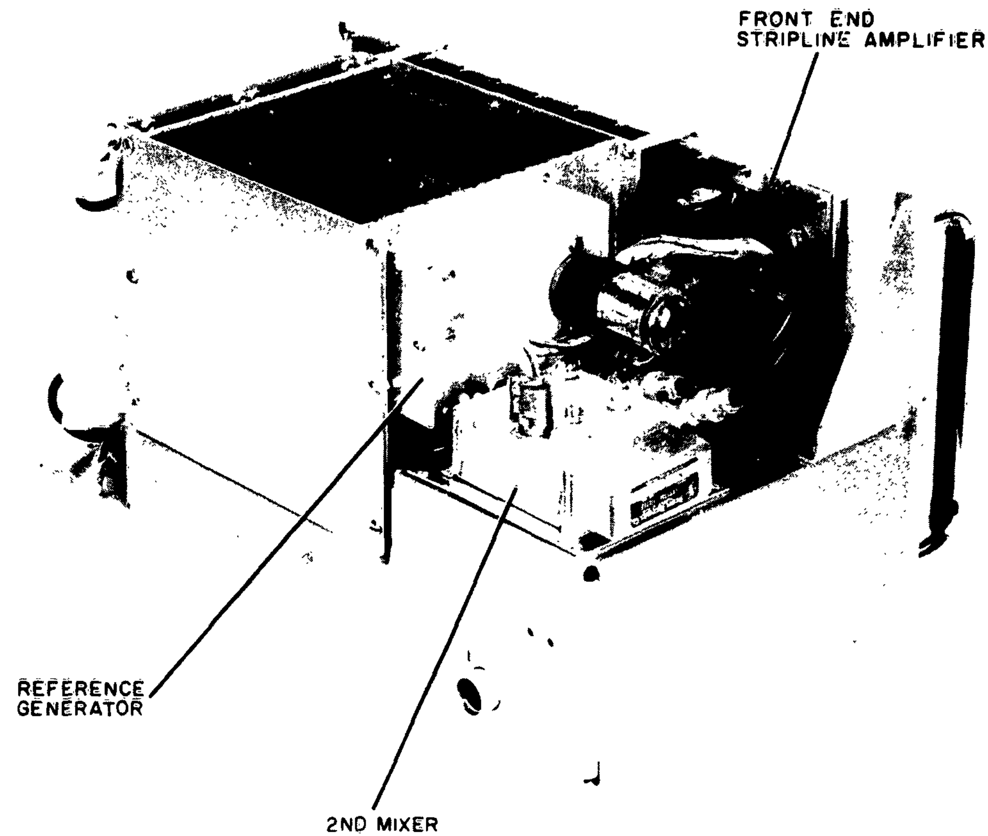


Figure 8. Solid State Tuning Device (Rear View)

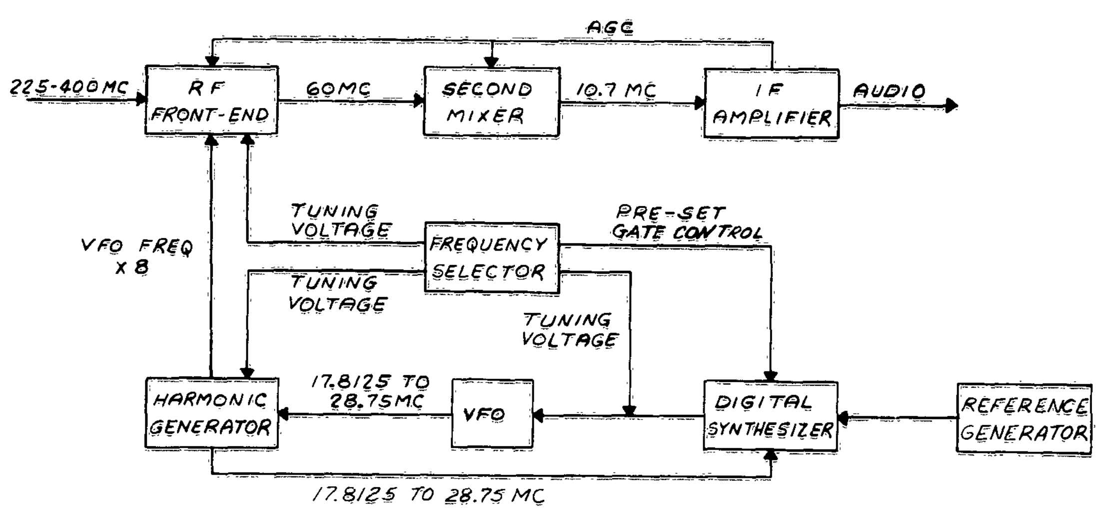


Figure 9. Solid State Tuning Device System Block Diagram

sufficiently to destroy the noise figure. It is expected that future improvements in varactor diodes will eliminate this problem.

No attempt was made to miniaturize the receiver unit. A conservative estimate is that it could be made in about one third its present size, which is 15 inches wide, by 8 inches deep and 9 inches high. Its present weight, which could be cut in half, is 20 pounds.

4.1 RECEIVER FRONT END ASSEMBLY

The function of the receiver front end assembly, shown in pictorial Figure 10, is to selectively receive amplitude modulated signals in the 225 to 400 Mc band from an antenna, amplify and convert them to a 60 Mc intermediate frequency, while maintaining a reasonable noise figure at the receiver input terminals. A block diagram of the front end assembly is shown in Figure 11. The electrical characteristics of the front end are listed below:

a. Tuning range — 225.0 Mc to 399.9 Mc in 100 Kc steps

b. Tuning method — electronic, by means of voltage variable capacity diodes

c. Input impedance — 50 ohms

d. Sensitivity — 8 microvolts for 10 db $\frac{S+N}{N}$ from 250 to 400 Mc. (See following paragraph, "Front End Assembly — Feasibility Model Performance Data").

e. Gain — 25 db

f. Image rejection — greater than 60 db.

A discussion of design consideration concerning Front-end circuit configuration is given in Appendix A.

A schematic diagram of the receiver front end assembly is shown in Figure 12. This description will follow the signal path through the assembly with special emphasis on portions of the circuitry that are of major interest in this program.

Amplitude modulated signals in the 225 to 400 Mc band are received from the antenna through coaxial jack J1. The input tank circuit consists of L1, CR1, C2 and C3. C3 is sufficiently large so as to be no appreciable part of the tuning capacity while providing a DC block for the varactor control voltage. CR1 is the frequency tuning device, with its capacity varying from 6 to 34 PF for a control voltage change of 110V to 1 volt. A more comprehensive discussion of CR1 and its operation are covered in the next paragraph. Capacitor C2 was added to parallel with CR1 to provide for tracking of the three front end tuned circuits on a single control voltage line. The signal input through C1, as well as the tank circuit output through C4 are impedance tapped on the

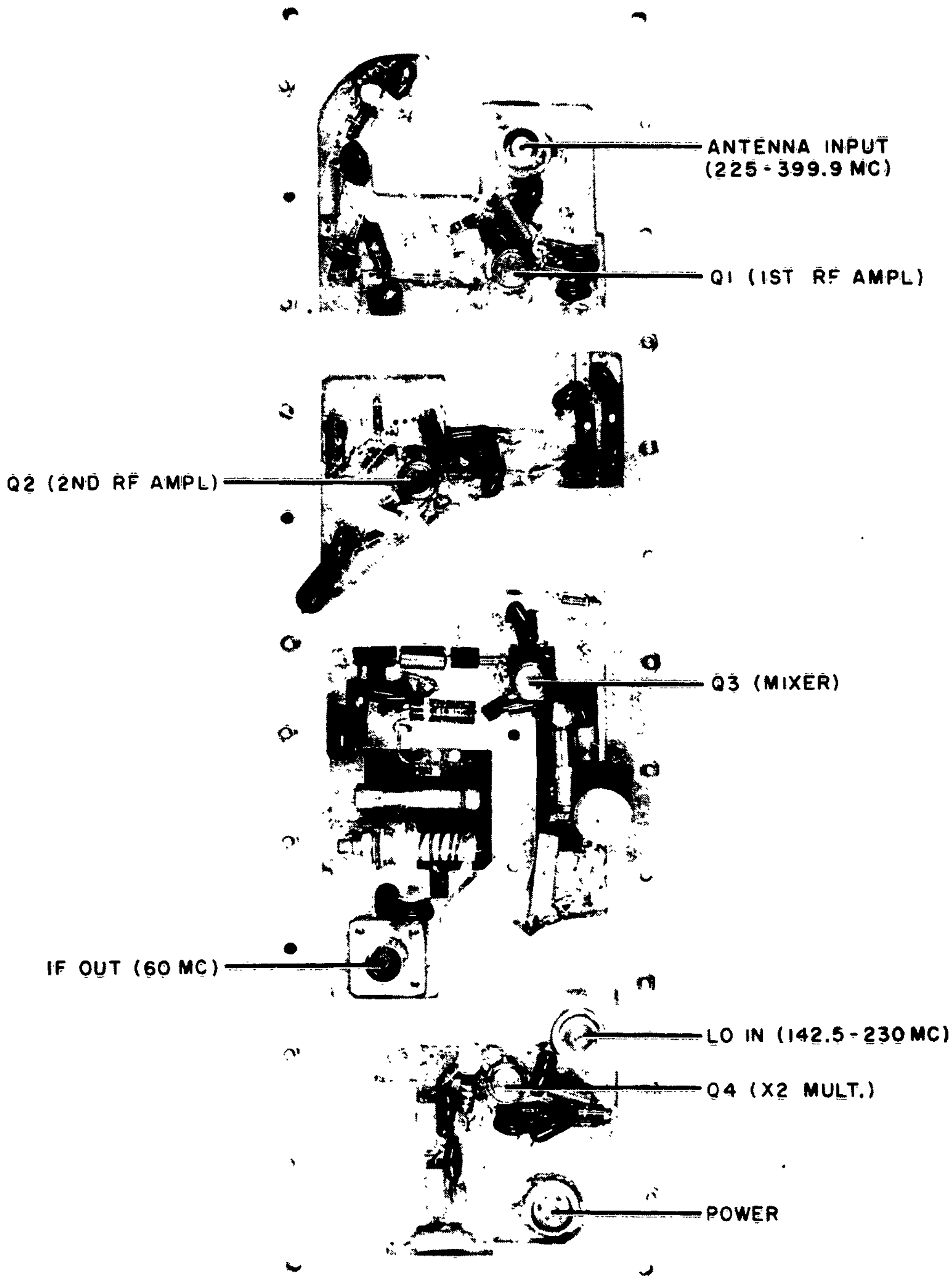


Figure 10. Front End Stripline Amplifier

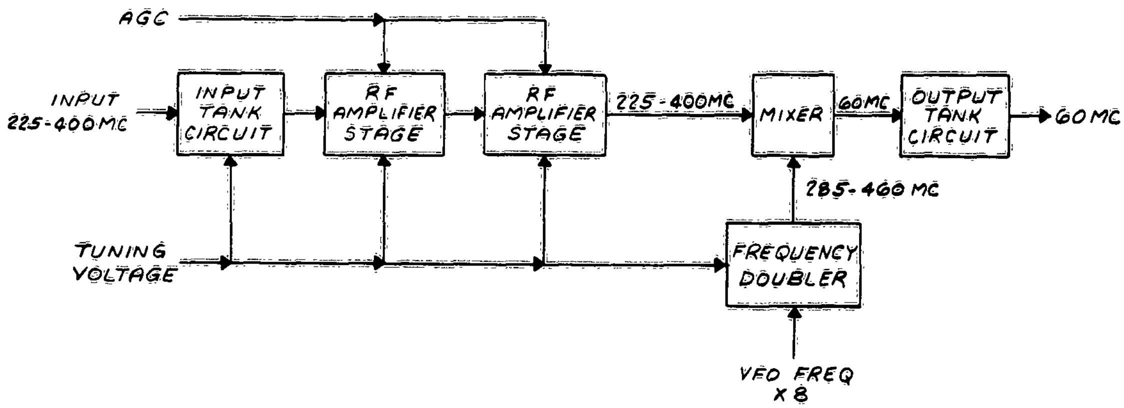
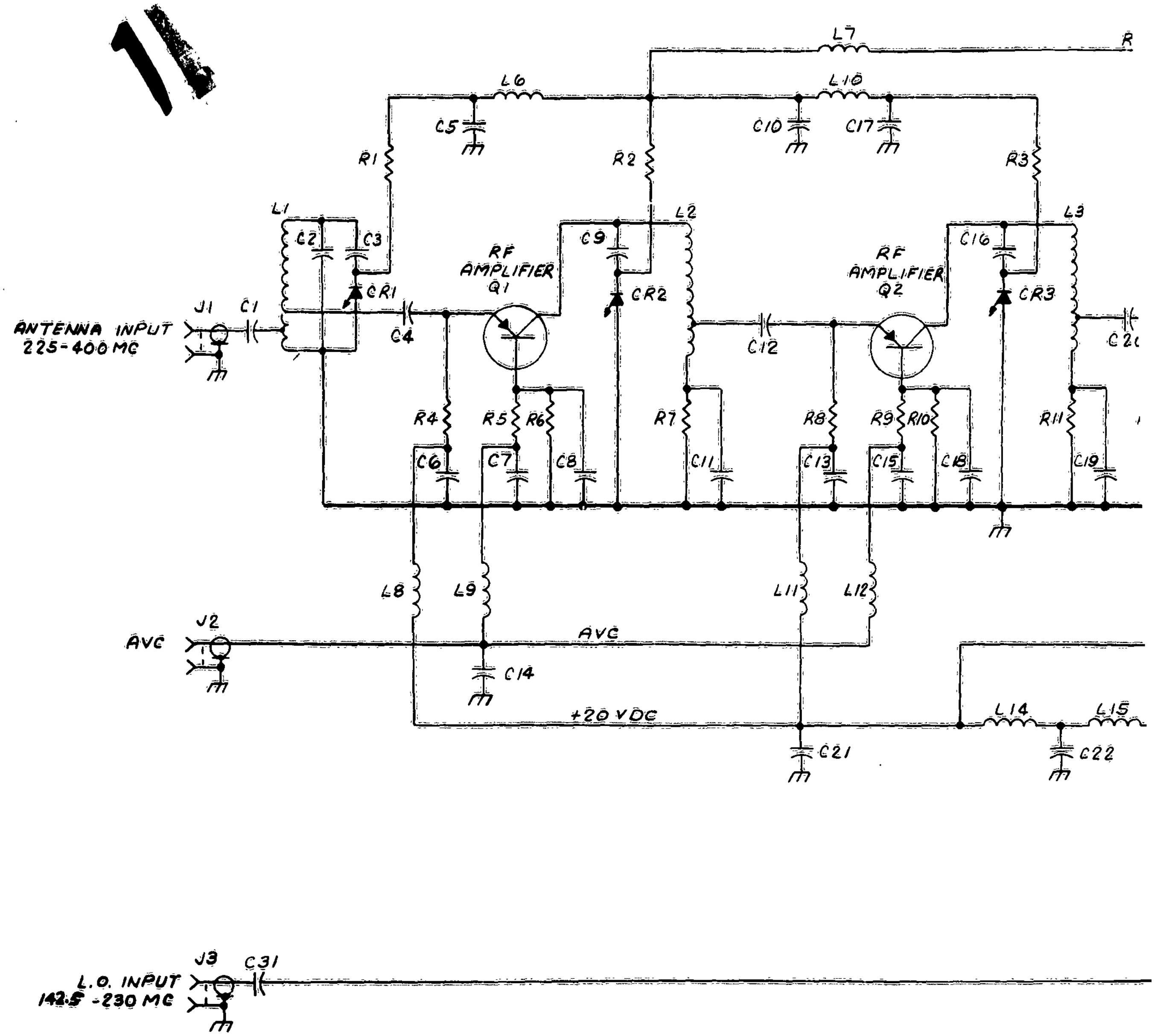


Figure 11. Front End Unit Block Diagram



ANTENNA INPUT
225-400 MC
J1
C1
L1
C2
C3
CR1
C4
R1
C5
L6
L7
R2
L10
C10
C17
R3
RF
AMPLIFIER
Q1
C9
CR2
L2
C12
RF
AMPLIFIER
Q2
C16
CR3
L3
R4
R5
R6
C6
C7
C8
R7
C11
R8
C13
R9
R10
C15
C18
R11
C19
L8
L9
L11
L12
AVC
J2
AVC
C14
+20 VDC
L14
L15
C21
C22
J3
C31
L.O. INPUT
142.5 -230 MC

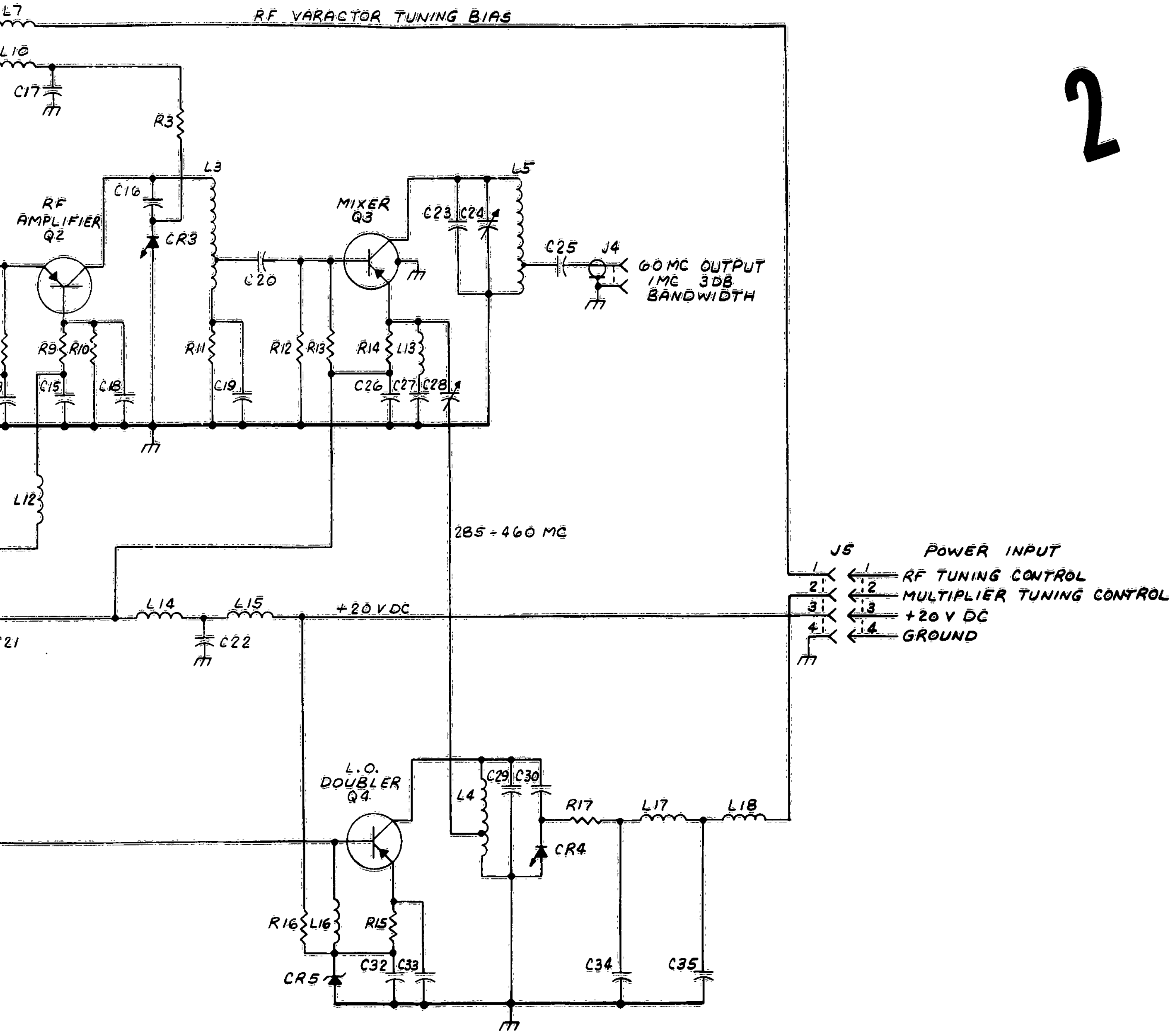


Figure 12. Front End Unit Schematic Diagram

inductance L1. The inductance L1 is in the strip-line assembly shown in Figure 10. Resistor R_1 is provided to limit the DC current through the varactor in case of diode avalanche. The components on the control line side of R_1 form a decoupling network.

Special consideration is given to the characteristics and performance of the diode, CR1 since it is a very important element in the electronic tuning system.

Numerous voltage variable diode capacitors are presently available on the commercial market. Many of these are referred to as varicaps, varactors, etc. The biggest single problem encountered in selecting a suitable diode was that of finding a component which would provide both the desired range of capacity and the necessary "Q" for tuning the 225 to 400 Mc band. A diode was obtained that offered the best available characteristic, however, it falls somewhat short of the desired characteristics. In order to provide the tuned circuits with "Q"'s of 30 necessary for image rejection, it is desirable to have all components Q's much higher than this value.

The Q of the varactor used is expressed by

$$Q = \frac{fc}{f} \quad \frac{\text{(figure of merit)}}{\text{Operating frequency}}$$

where fc is a figure of merit defined as $fc = \dfrac{1}{2\pi \text{ Rs C min}}$

Rs is the diode series resistance, and C min is the diode capacity at breakdown voltage. Values of Rs and C min for the diode used provide a capacity Q of 39 at 400 Mc which degrades to a Q of 11.8 at 225 Mc. This degradation of Q in the low end of the band results in a loss of receiver sensitivity in that region. Manufacturers of the diodes suggest that components will be available in the near future that will permit tuning of the entire range without loss of sensitivity. The voltage characteristic necessary to tune the diode in the circuit cannot be accurately calculated, since it is dependent to some extent upon stray capacitance and inductance. Examples of tuning voltage vs. frequency curves for the receiver front end may be found in Figures 13 (A, B, and C). The functions shown in these graphs are approximately fourth order. They were derived from actual measurements in the front-end circuits. The voltage function necessary for tuning is developed by a combination of precision voltage dividers and decade switches, described in paragraph 5.5 of this report.

The RF amplifier Q_1 is a type T2028 transistor selected for this purpose on the following considerations:

a. The T2028 can deliver approximately 10 db of gain and has a 10 db noise figure at 400 Mc.

b. It has a forward AGC characteristic that provides good gain control over a wide range of signal input levels.

c. It is relatively inexpensive and is readily available.

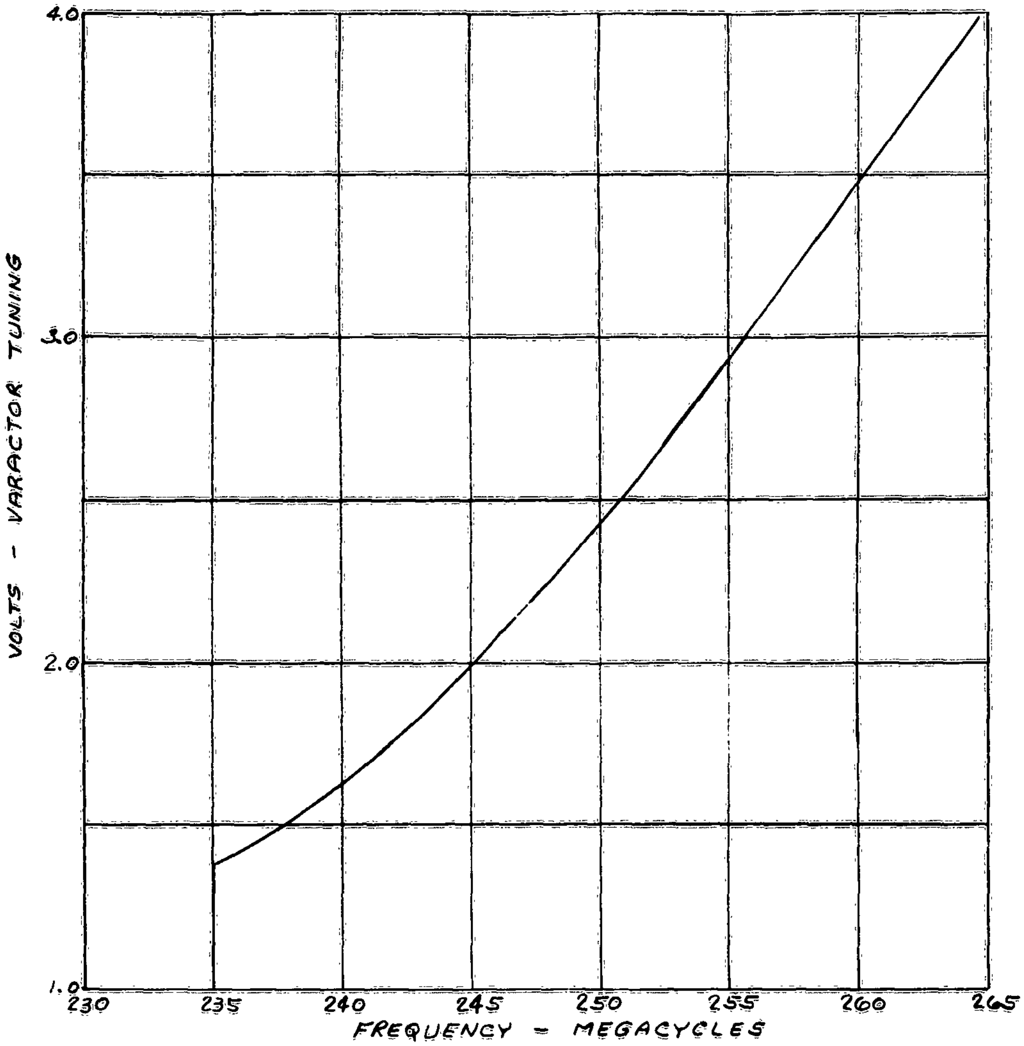


Figure 13(A). Varactor Tuning Volts vs Frequency

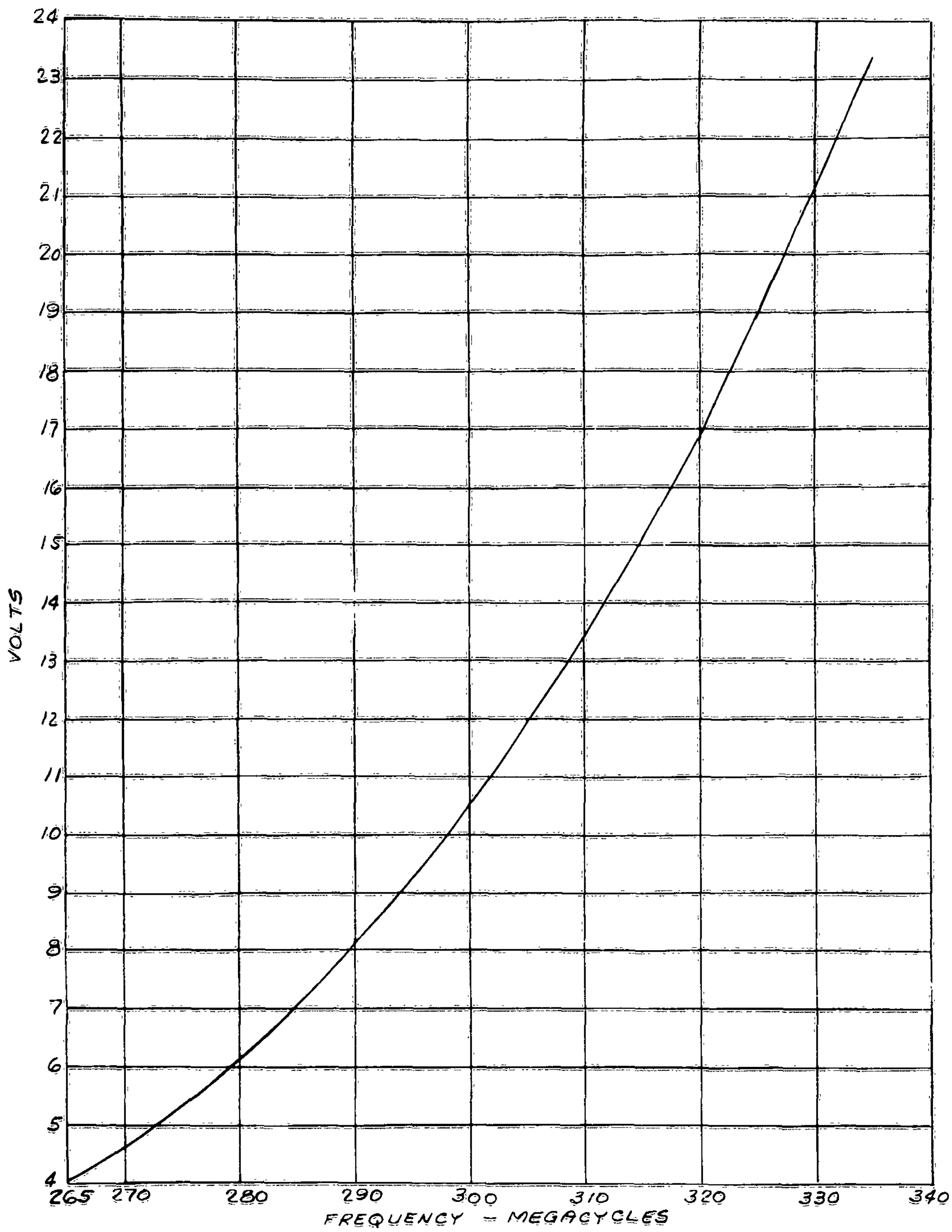


Figure 13(B). Varactor Tuning Volts vs Frequency

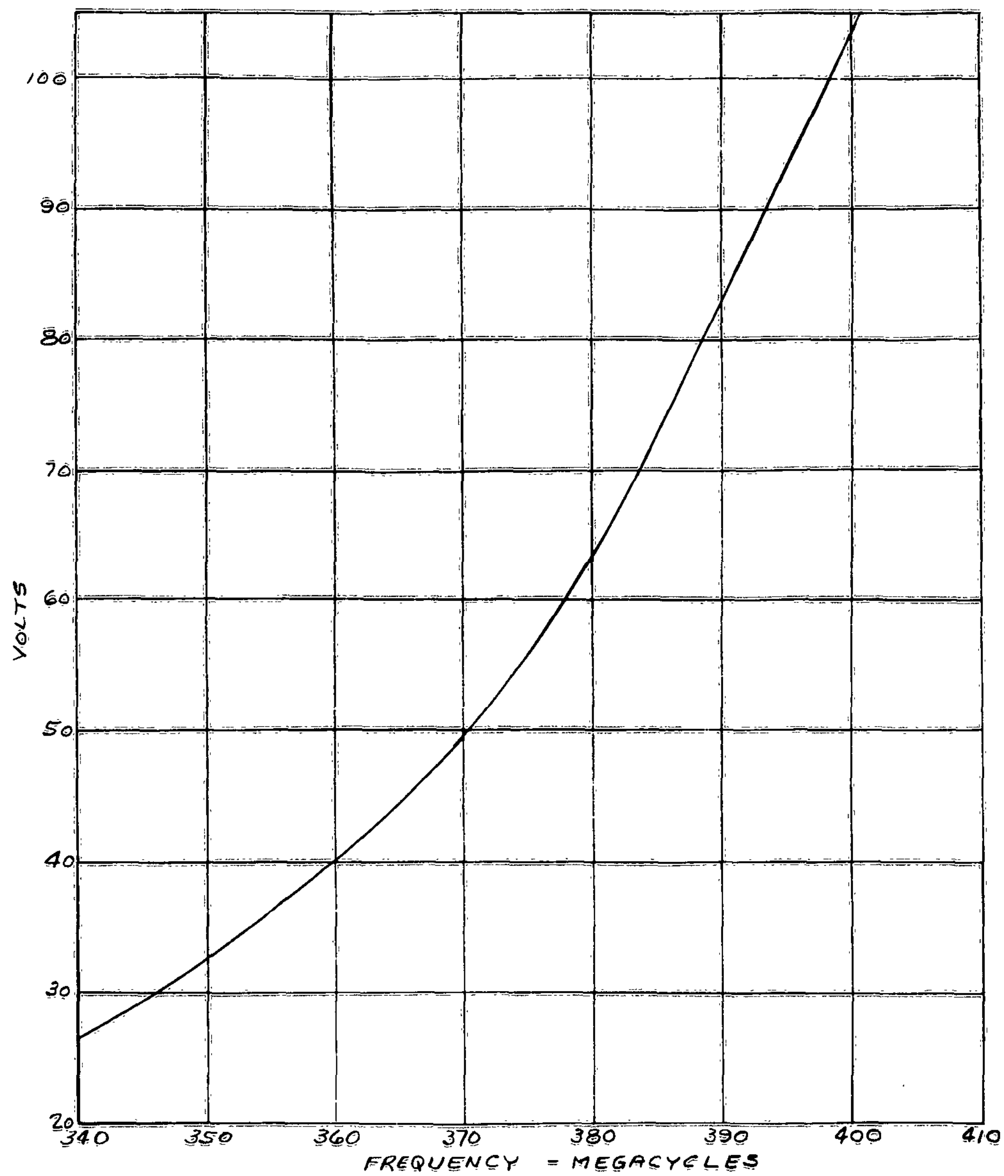


Figure 13(C). Varactor Tuning Volts vs Frequency

The RF amplifiers Q_1 and Q_2 are operated in the common base configuration to obtain maximum gain at 400 Mc. Attempts were made initially to operate the transistor in the common emitter configuration; however, it was found that the lead inductance in the emitter could not be properly bypassed and degeneration reduced gain. A scheme for tuning out the inductance with a series capacitance was investigated. The capacitor could be adjusted to produce sufficient gain over a narrow band of frequencies. It did not, however, perform satisfactorily across the 225, to 400 Mc band since, to be effective it must be a narrow band device.

AGC action may be obtained by either of two methods, reverse AGC or forward AGC. For this application, the forward AGC mode was selected. A comparison of the two modes will indicate the reasons for this selection. Figure 14 illustrates the two circuit configurations. In the forward mode, a resistor is placed in series with the cold end of the tank circuit. As the amplitude of the input signal increases, AGC voltage is applied to drive the transistor base more negative, thereby causing the transistor to conduct harder. As the collector current increases, the voltage drop across the collector resistor increases causing the collector to emitter voltage to decrease with a resultant reduction in gain. The second method of AGC, (reverse AGC) is accomplished in the usual manner by biasing the transistor off. While there is a greater center frequency shift and bandwidth variation with forward AGC, this condition is overshadowed by the superior overload characteristics of forward AGC. When reverse AGC is employed, the overload level decreases as the gain decreases, whereas with forward AGC the overload level increases as the gain decreases. Forward AGC provides approximately 100 times better overload performance than reverse AGC. The use of forward AGC presented a problem in construction of the actual circuit. It may be seen from the circuit diagram in Figure 14(B) that the ground point of the resonant circuit must be provided by capacitive bypassing rather than by direct grounding. It therefore becomes necessary to select a capacitor which does not appear inductive at any point in the 225 to 400 Mc frequency band. The capacitor selected for this purpose was a special disc type connected into the circuit such that the stripline inductance connects directly to one side of the capacitor and the ground plane connects to the other. This configuration virtually eliminates all lead inductance and was found experimentally to produce the best by-passing.

RF Amplifier stage Q_2 operates in a manner similar to that of the first stage Q_1. The two stages produce a gain of approximately 20 db.

A type T2029 transistor was selected for the mixer stage. A discussion of the types of mixers considered is given in appendix A of this report. Local oscillator drive of 1 mw is supplied from the L0 doubler stage Q4 thru impedance matching capacitor C28. The serious circuit of L13 and C27 is a 60 Mc trap provided to present a very low impedance to 60 Mc in the emitter circuit. If the mixer is to have conversion gain, it is important that a low

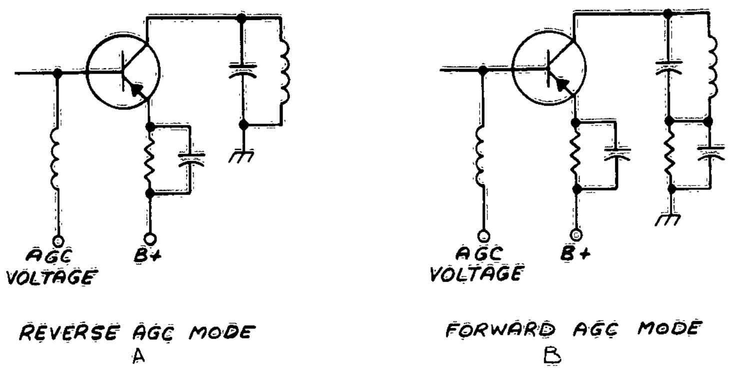


Figure 14. AGC Modes

impedance to 60 Mc be obtained in the base circuit also. A trap similar to the one used in the emitter was tried in the base circuit. It was found that the trap could be tuned to produce mixer conversion gain over a narrow band of signal frequencies, but at some point in the 225 to 400 Mc band it would cause the mixer to become regenerative. It was found that if the coupling capacitor C20 was physically situated so as to provide a direct connection (practically no lead length) between the mixer base and the tap on the stripline, then a very low impedance to 60 Mc was provided. While this impedance varies with frequency, the change is minor and eliminates the problem of regeneration. The output circuit of the mixer is a 60 Mc resonant circuit with a 1 Mc 3 db bandwidth. The inductance L5 is tapped to provide a 50 ohm output impedance.

The mixer noise figure is optimum when the transistor is operated at a collector current of .5 ma and is supplied with 1 milliwatt of L0 drive. It was determined that the L0 drive could vary from .8 mw to 1.5 mw without degrading the noise figure appreciably.

The last L0 doubler stage was included in the front end assembly since its frequency range (285-460 Mc) is better suited to the stripline construction of the front-end than the lumped circuit construction of the harmonic generator. The doubler is tuned across the required band with a varactor of the same type used in the RF amplifier circuits. The tuning voltage is obtained from the harmonic generator control line. A more detailed description of the operation of the doubler stages may be found in the harmonic generator paragraph 4.4 of this report.

Experimental work indicates that all of the components included in the front end assembly can be replaced without the need for retuning. Data indicates that while the tuning characteristics of the varactors are slightly different, they are similar enough to provide tracking across the band. It was also found that closer tracking could be provided, if desired, by operating each varactor from a potentiometer connected to the control line.

Front End Assembly-Feasibility Model Performance Data:

The feasibility model of the front-end was constructed in stripline and tested in the system with the following results:

a. Tuning range: The front end can be continuously tuned through the 225 to 400 Mc band solely by the use of voltage variable capacity diodes and without the need for bandswitching or mechanical tuning.

b. Sensitivity: The front-end exhibits a 8 uv sensitivity for a 10 db S+N/N at frequencies between 250 and 400 Mc. Sensitivity below 250 Mc is degraded to approximately 30 uv for 10 db S+N/N at 235 Mc. The reason for this loss in sensitivity is that the Q of the tuning varactors is degraded in that region. An explanation of this loss of Q is given on page 23 of this report. It is felt that as better varactors become available this problem can be eliminated.

No special components were used in the front end assembly with the exception of capacitors C11, C19, which are a special disc type with minimum lead inductance. All other components are of standard military types. The varactors used are type MA4358F and are available from manufacturers stock.

4.2 DIGITAL SYNTHESIZER

The function of the digital synthesizer is to operate in conjunction with the VFO to provide the 1750 discrete local oscillator signals required for 100 Kc channel spacing. To accomplish this, the synthesizer samples the VFO frequency and divides it by a pre-set number in order that it may be phase compared to the reference generator. It then generates a control voltage related to the phase difference of the two signals, and applies it to the tuning elements in the VFO so as to correct its frequency and maintain a phase locked condition between the VFO and reference generator.

The overall goal is to produce a signal whose frequency is determined by a given discrete combination of switch positions. It is further required that a large number of frequency channels be readily available. It is highly desirable to have the control knobs indicate the carrier frequency directly in either a transmitter or receiver, without the necessity of translation by the operator. It is usually desired to divide the tuning range of a communication system into a number of constant bandwidth channels. This, in effect, requires that the channels be spaced in an arithmetic progression, in order to make most efficient use of the allotted tuning range.

The use of switched crystals is a solution; but this is rather complex and expensive, especially if the number of channels is large and a high accuracy is required. Crystal saver techniques require fewer crystals; but require mixers which introduce problems of tuning and spurious responses. A simple approach would be to simply multiply the desired frequency using one crystal and a harmonic multiplier. Unfortunately, there is no practicable way to obtain high, prime number multiplication ratios. There is a method to divide a frequency by any integer in which high prime numbers are no more difficult than any other number.

The use of a frequency divider suggests the possibility of a feedback control loop consisting of a frequency divider, a voltage tuned oscillator and a suitable error detector. The most obvious error detector might appear to be a frequency discriminator. The resulting control system is then merely a simple regulator in which an error must exist before correction can take place. The magnitude of the error is a function of the open loop gain. The principal deficiency of this scheme is that a steady-state frequency error can exist; for there must be an error in order to apply a corrective voltage to the oscillator.

The deficiencies of a simple frequency sensitive detector can be overcome by using a phase sensitive detector which compares the phase of the counter output with that of a reference frequency derived from a crystal oscillator. In such a system, the frequency error is effectively integrated with respect to time. The integration is inherent to the system because frequency is the rate of change of phase. In this system, the steady-state frequency error is zero because any steady-state error in frequency would result in a steadily increasing phase error, which would lead to a correction. The phase sensitive detector system can have a steady-state phase error, or a velocity-lag error in frequency; but these are not serious problems in the intended application.

The counter used must be adjustable and a true frequency divider, capable of recycling without lost time at the end of the count. Such a counter may be devised by dividing it into two parts, with appropriate transfer gating, so that the count is alternately transferred from side to side. The total count to completely cycle the counter is then the sum of counts in the two sides. The division is adjusted by presetting one side during its non-counting period. Such a counter is shown in Figure 15. The blocks labeled A, B, B, and C, (Figure 15), constitute the preset side. The blocks labeled D, E, and F, (Figure 15), constitute the fixed side. The flip-flop and gates in the H block affect the count transfer, while the single-shot and pulse amplifier produce the preset pulse. The preset number is controlled by the tuning knobs.

The exact details of proportioning the counter depends upon the number of channels and IF frequency offset. As an example, the UHF receiver which was built will be considered. This receiver must tune from 225.0 to 399.9 Mc. The IF frequency is 60.0 Mc. The oscillator is specified to operate on the high side of the signal in order to reduce the high to low end frequency range. The channel spacing is 100 Kc.

The above specification requires that the local oscillator signal, injected at the mixer, must vary from 285.0 to 459.9 Mc in 1750 steps of 0.1 Mc. Since it is beyond the present state-of-the-art to construct a suitable counter to operate directly at these frequencies, a harmonic multiplier was used to multiply the VFO frequency to the requred value. The present practicable limit to the counter frequency is approximately 30 Mc. A simple division shows that the harmonic multiplier must multiply by a number greater than $459.9/30 = 15.3$. It is also an important practical consideration that the harmonic multiplier ratio be a number composed entirely of factors of two and three, since doubling or tripling are relatively easy. Ratios of 16, 18, 24, 27, and etc. are suitable. A ratio of 16 was chosen because it is composed of four doublers. The required VFO tuning range is then $285.0/16 = 17.8125$ Mc to $459.9/16 = 28.74375$ Mc. One channel frequency change at the VFO is then: 100 Kc/16 = 6250 cycles per second, which is the correct reference frequency.

It now becomes convenient to think of the synthesizer in terms of channels. Let the over-all divisor number be designated N. The action of the servo loop is such that the VFO frequency is adjusted so that dividing the VFO frequency by N exactly equals the reference frequency. This is equivalent to saying that the VFO frequency is N times the reference frequency. In the example the reference frequency corresponds to one channel. The range of N is from 2850 to 4599 for a dial setting of 225.0 to 399.9 respectively.

In order to make the proper translation for the dials to read the carrier frequency directly, it is desired to have the three least significant dials read in a decimal fashion. The most significant dial must read only two positions. In Figure 15, the blocks labeled A and the two blocks labeled B must therefore be decades. The block labeled C may be an ordinary binary counter of sufficient size.

Also in order to make the proper translation of 600 channels offset, the side of the divider made up of blocks D, E, and F may form a scale of 600, 1600, or 2600. The significance of these numbers is that block C counts in thousands of channels. The entire left side must pass from a number ending in 999 to the next even thousand as the dials are changed from 299.9 to 300.0. This can be accomplished by forcing the units, tens, and hundreds of offset channels into the right hand side. Of the choices of counts in the right hand side, 600 is desirable because it requires a minimum of hardware and still allows sufficient time for presetting. Making block C a total of four counts will give a total of 4000 + 600 = 4600 counts total, which is sufficient.

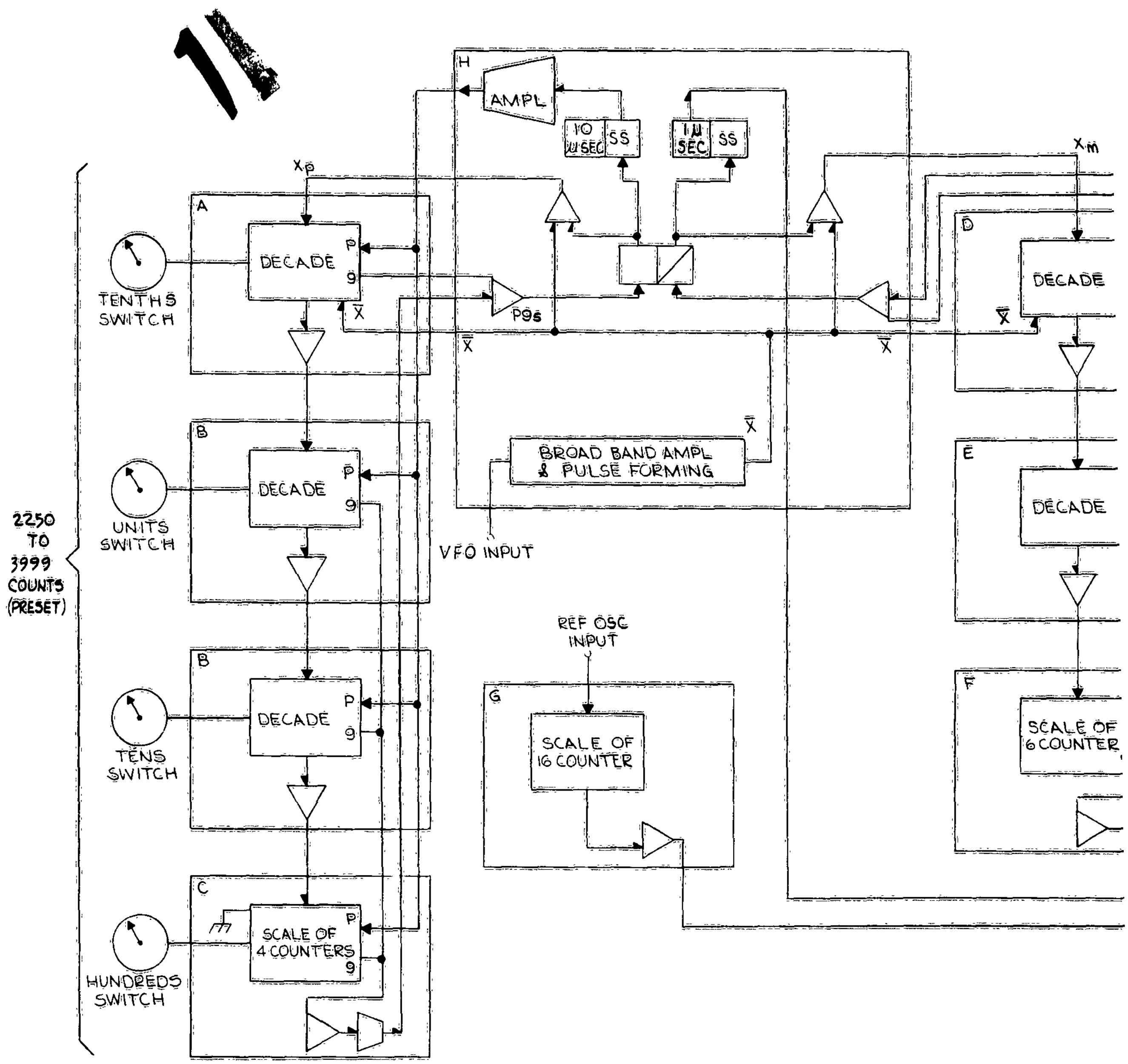
The count transfer is accomplished by a gating arrangement in block H. Suitable "9's sensing" coincidence gates affect the transfer when the left side reaches the count of 3999. The return is made when the right hand side reaches 599. These numbers are of great significance due to several unusual properties. These numbers are respectively one count less than the count which changes the entire side to zero. These numbers are obtained with the absolute minimum propagation delay through the counter. This is of great importance for the gating must occur in less than one count interval. The choice of these numbers makes the dial translation perfect, as will be illustrated.

Suppose the dials are set on a number D, in megacycles. The correct value of N is:

$$N = 10\,D + 600$$

Let the left hand side be preset to a number, P. The left side then counts 3999-P counts. The right hand side counts one complete cycle from 599 to 599 or 600 counts. The sum of the two is equal to N. Thus,

$$N = 3999 - P + 600.$$



H
AMPL
10 µSEC
SS
1 µ SEC
SS
Xp
Xm
A
DECADE
P
9
X̄
P9s
D
DECADE
TENTHS SWITCH
BROAD BAND AMPL & PULSE FORMING
B
DECADE
UNITS SWITCH
E
VFO INPUT
2250 TO 3999 COUNTS (PRESET)
REF OSC INPUT
G
SCALE OF 16 COUNTER
TENS SWITCH
F
SCALE OF 6 COUNTER
C
SCALE OF 4 COUNTERS
HUNDREDS SWITCH

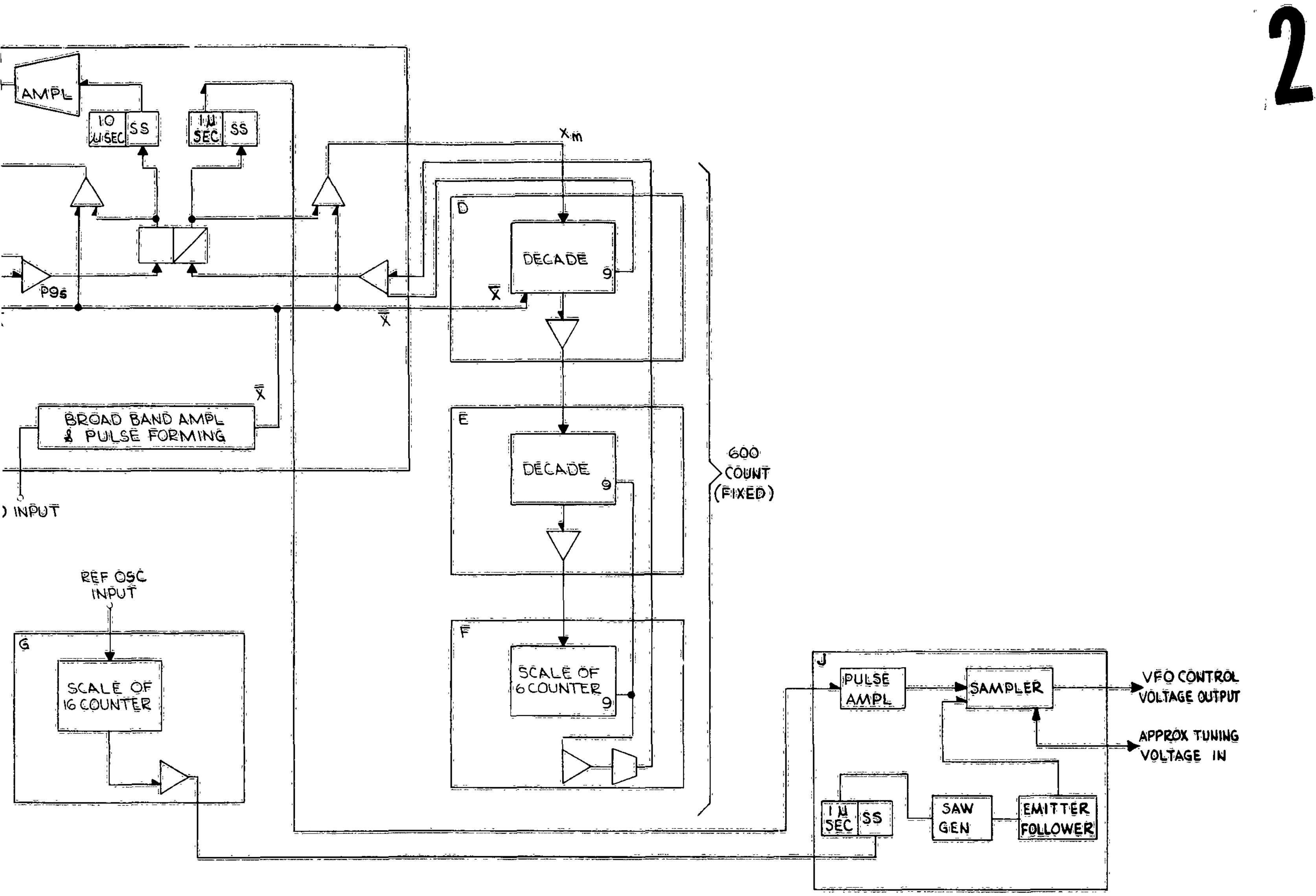


Figure 15. Digital Synthesizer System Block Diagram

Equating the above two expressions for N gives:

$$10D + 600 = 3999 - P + 600.$$

Solving for P:

$$P = 3999 - 10D$$

It is apparent that subtracting any smaller number from 3999 results in no carries (or borrows). The presetting is then very easy. Each counter block has a corresponding switch. For the three least significant dials, subtracting that dial number from nine yields the preset number in the corresponding decade. For the most significant dial, subtracting that dial number from three yields the preset number in the scale of four counter in block C.

It should be noted that the design of the digital frequency divider and solving the dial translation problem is a straight forward arithmetic exercise. The right hand portion in the example was obtained using feed-back counters because it was convenient. If a similar presetting arrangement were made on the right hand side, any integral number of channel offset could be used. By suitable switching of these right hand side presets, a transmit-receive synthesizer or a high-low offset is possible. Fractional channel off-setting can be attained if the offset is a rational number of channels (602 1/4, for example, by multiplying N by four and causing the least significant dial to stop only every four counts). Finally, in certain cases the right hand side might be a simple binary chain for certain offsets. The purpose of these examples is to emphasize that the design of the particular synthesizer described in the foregoing is not based on an obscure numerical oddity. The offset of 600 channels is convenient; but not unique. The division scheme can be found by a straight-forward process for any number of channels and any rational number of channels offset, including zero and negative offsets. A practical limitation to observe is that on either side the minimum count must allow adequate presetting time.

The entire digital portion of the synthesizer was built on ten plug-in boards similar to Figure 46. (Figure 46 is located in Appendix C. See List of Illustrations for page number.) Seven boards make up the two portions of the frequency divider. There is one control board (block H), a scale of 16 counter to derive the 6250 cycle reference frequency from a 100 KC crystal oscillator (block G) and a phase detector card "J" shown in Figure 15.

The phase detector card consists of a pulse amplifier to generate a 20 volt sample pulse at the end of the VFO counter cycle. The single-shot, sawtooth generator, and emitter-follower produce a low impedance sawtooth waveform in synchronism with the 6250 cycle per second reference frequency. The sampler is a bilateral gate so arranged that the pulse samples the sawtooth waveform. Provision is made to add the approximate VFO tuning voltage, which is derived from the frequency control switches and a voltage divider. The capacitor stores the sample voltage between corrections.

The overall function of the phase detector card is to add, or subtract, the necessary correction to the approximate VFO tuning voltage to produce the exact VFO tuning control voltage required. This was accomplished by using a pulse generated at the completion of one cycle of the VFO frequency divider to sample a sawtooth waveform generated by the 6250 cycle per second reference signal. This sample voltage is stored in a capacitor to maintain a constant control voltage between samples. The relative phase between the start of the sawtooth waveform and the occurrence of the counter pulse determines the sample voltage and thus the control voltage during the following interval. If the VFO frequency is low, sampling occurs later, and at a higher voltage, than the previous sample. This raises the VFO frequency during the following interval. A similar action occurs to lower the VFO frequency, when necessary. The VFO control voltage follows a series of steps which converge on the exact value. The condition of phase-lock occurs when sampling repeatedly occurs at the same voltage. The advantage of this type phase detector is that the need for correction is immediately recognized and the correction process started. Once phase-lock occurs, the steps in the control voltage become imperceptably small. This permits fast correction, a wide lock range with respect to voltage, and low ripple content.

In the digital portion voltage and component tolerances were considered. Although this portion might appear complex, past experience has shown similar circuitry, to be highly reliable, in even more complex systems. The use of modular construction or similar techniques would make it possible to meet severe environmental and mechanical specifications.

A detailed discussion of the circuits, methods of testing, and the solution to some minor problems encountered can be found in Appendix C.

4.3 VARIABLE FREQUENCY OSCILLATOR

The variable frequency oscillator shown in Figure 16 is the basic local oscillator for the receiver. Its function is to generate any of 1750 pre-set frequencies between 17.8125 and 28.75 Mc.

These signals are multiplied by a factor of 16 and become the local osicalltor signals for tuning the 225 to 400 Mc band in 100 Kc steps. The VFO is located electrically in a phase locked loop (Reference Figure 9). The oscillator circuit is a Colpitts type and is tuned by means of voltage variable capacity diodes. The tuning voltage is determined by the combination of a pre-set voltage and a variable voltage provided by the phase lock circuitry. A detailed explanation of the phase lock circuits may be found in paragraph 4.2 of this report.

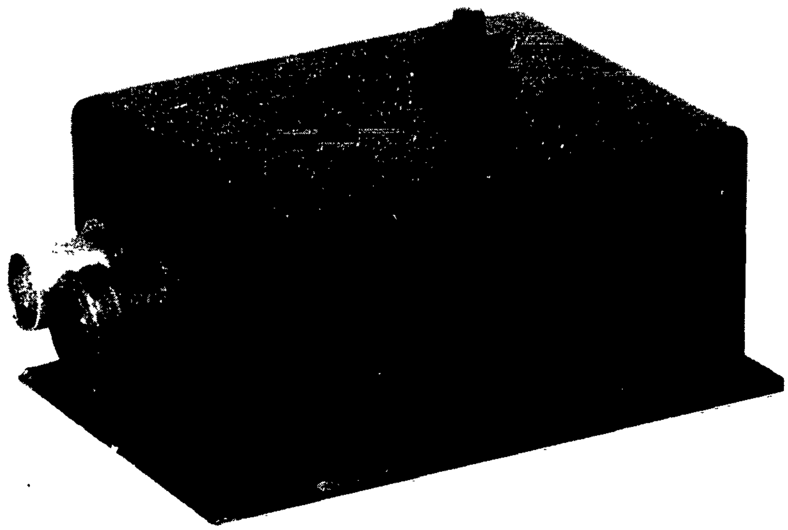


Figure 16. Variable Frequency Oscillator

VFO Characteristics:

a. Tuning range -17.8125 Mc to 28.750 Mc

b. Tuning mechanism - voltage variable capacity diodes

c. Output Level - 60 mv across 50 ohms

d. Frequency stability - refer to page 58.

A schematic diagram of the VFO is shown in Figure 17. A description of the circuit operation is as follows: The circuit is a Colpitts VFO utilizing variable capacity diodes as the tuning elements. Two diodes are operated in parallel to minimize the tuning effect of transistor collector capacitance. This collector capacitance varies with temperature; consequently it has an appreciable effect on tuning when the varactor is operated at minimum capacity (6 uuf). By paralleling two diodes, the minimum diode capacity is doubled, thereby reducing the effects of collector capacitance. The transistor is biased such that the collector o base voltage is less than 3 volts. Although this low voltage reduces the gain of the transistor and degrades stability somewhat, it is a necessary condition for providing the proper tuning range. In order to tune the 17 Mc to 28 Mc band, the varicap control voltage must swing from +3V to +120V.

The diode must remain in its reverse-biased state, hence, the peak AC voltage swing at the collector of the transistor must remain lower than the 3-volt control voltage minimum. This prevents rectification of the AC by the varactor which would cause self biasing. The oscillator is lightly coupled to a buffer amplifier stage which provides 80 mv ±1.5 db of signal into 50 ohms. The buffer circuit was made a part of the VFO assembly since it is advantageous to have the VFO isolated completely from the external cabling. The buffer insures that impedance variations in the cables or circuits driven by the VFO will not affect its operating frequency or stability. A zener diode circuit is provided to maintain a regulated supply voltage for the oscillator. Decoupling networks are provided for both the +20 volt supply line and the varactor control line. It should be noted that the control line decoupling circuits are designed for filtering high frequencies only, such that they do not present any appreciable phase shift in the control loop response.

Frequency Stability:

The VFO is required to have both amplitude and frequency stability. Amplitude stability is required for two reasons: (a) The amplitude of signal provided for the digital portion of the circuitry must remain fairly constant to insure phase locking; (b) The amplitude of the signal provided for the multiplier must remain within 1 mw ±1.5 db in order that the signal mixer will have the proper local oscillator drive level.

Frequency stability is required to maintain accurate 100Kc channel tuning and to prevent FM distortion in the IF Amplifier. This distortion develops as follows:

> Frequency deviations of the VFO will produce IF carrier deviations which are equal to the product of the multiplication factor of the harmonic generator (16) and the frequency deviation of the VFO. If the IF bandpass, for example, were perfectly flat over the 32Kc center portion, then a VFO deviation of ±1Kc or less would produce no FM distortion in the receiver output. A typical IF bandpass for 100 Kc channel spacing is shown in Figure 18. Considering a 30 percent audio modulation and selecting a minimum desired audio signal to noise ratio of 30 db, the AM produced by carrier shift cannot exceed .95 percent. The maximum slope within the pass band is about .0037 percent modulation per cycle. At this point of maximum slope, a carrier shift of 256 cycles produces a .95 percent amplitude modulation. Since the local oscillator frequency is multiplied by 16, the permissible VFO shift is 256/16 = 16 cycles of ±8 cycles. Several causes of frequency variations in the VFO are listed in the following paragraphs. With each cause a discussion of the steps taken to reduce or eliminate the variations is given.

Temperature as a cause of frequency variation:

Temperature variations produce changes in the capacitance and inductance of circuit components with a resultant change in oscillator frequency. Capacitors which are within or connected to the oscillator tuned circuit such as C 1, 2, 3 in Figure 17 were selected from high grade ceramic capacitors that have small percentage variations with temperature. Temperature compensated capacitors would be best suited for this case; however, they were not readily available at the time of VFO construction, in the values required. Also, some amount of variation can be tolerated since it will be compensated for by the action of the frequency control loop. The amount of variation that can be tolerated is determined by the ability of the control circuit to lock the VFO within a normal range of temperatures. The inductance in the tuned circuit was formed on a Rexolite rod and encapsulated in a material with properties similar to that of Rexolite to minimize inductive tuning with temperature. The greatest tuning effect with temperature is contributed by the transistor. Since the transistor is operated at reduced gain in order to minimize varactor rectification of the AC signal, its variation in gain with changing temperature is aggravated. Changes in gain produce changes in transistor collector capacitance. Since the transistor collector capacitance is directly in parallel with the tuned circuit, changes in this capacitance have a direct effect upon frequency. This effect was reduced by placing two varactors in parallel, such that their combined minimum tuning capacitance (12 uuf) is much greater than the change in collector capacitance. The change in capacitance of the varactors with

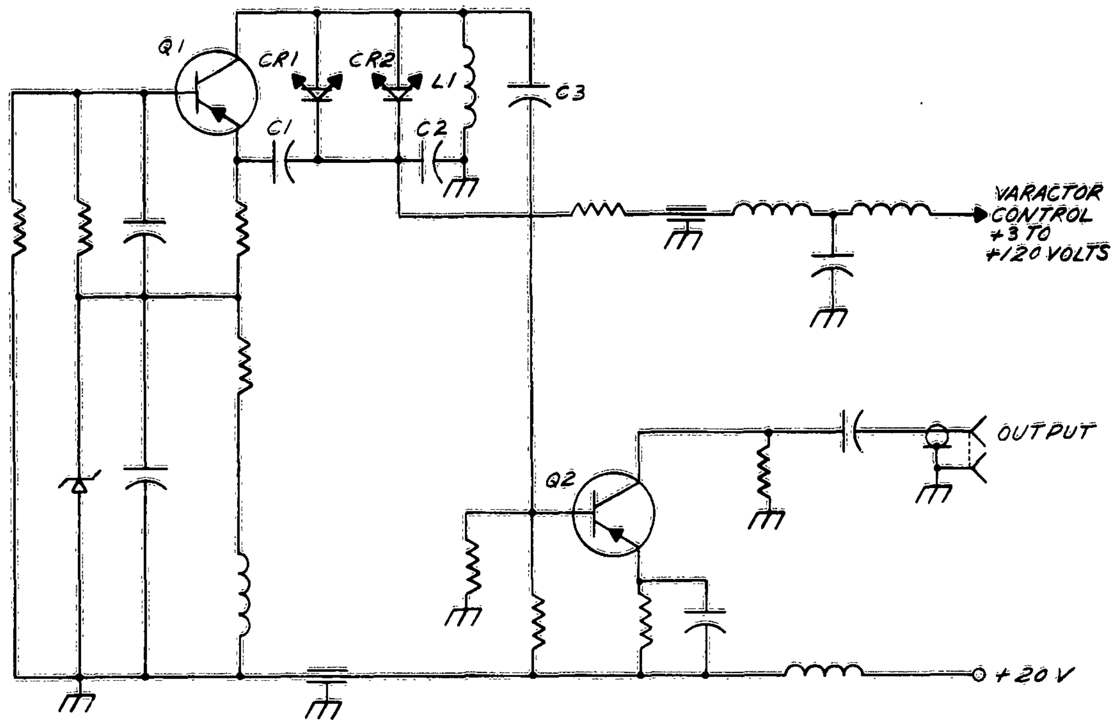


Figure 17. VFO and Buffer Amplifier

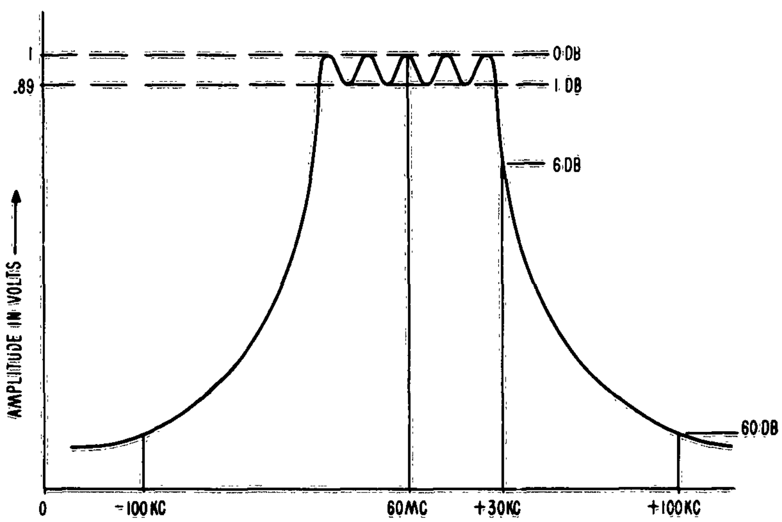


Figure 18. IF Band Pass

temperature is negligible over the selected range of 0° to 50°C and they were therefore left uncompensated. The effect of temperature upon VFO frequency is shown in a graph, Figure 19. It can be seen that the average frequency change in the VFO with temperature from 0° to 50°C is approximately ±300 Kc with the worst case (±500 Kc) occurring in the 28 Mc region. One requirement of the phase lock system is thereby established; it must have sufficient voltage-lock range (approx. 20V) to hold the phase lock condition across the frequency band.

Voltage variation as a cause of frequency variation:

Frequency deviations in the VFO may occur from changes in either supply voltage or varactor control voltage. Changes in supply voltage will result in a change in transistor gain and collector capacitance, with a resultant frequency deviation. To eliminate such occurrences, the regulated +20 volts from the power supply is further controlled by a 12 volt zener circuit within the VFO chassis. Test indicate a maximum change of ±2 Kc at 17Mc will occur for a ±1 V change at +20 V. The change decreases to ±1 Kc at 28 Mc. The most significant changes in frequency due to voltage variations are caused by variations on the varactor control line.

Figure 20 shows a graph of frequency vs. control voltage for the VFO. It can be seen that the greatest effects of voltage variation upon frequency are obtained at the lower end of the frequency band. In the 17.2 to 18 Mc region the tuning function is equal to 750 KC/volt or 750 cy/Mv. Therefore, a 1 mv change in the DC control line will produce a carrier deviation in the IF equal to (750 cps x 16) or 12 Kc. To minimize this effect, a well regulated low ripple supply was designed and fabricated. It should be pointed out that any changes in the supply voltage that occur at frequencies within the control loop response will be reduced by the action of the loop.

Shock and vibration as a cause of frequency variation:

All components and leads within and surrounding the tuned circuit were rigidly mounted to prevent changing lead to chassis capacitances and changing inductance in the tuning coil. Several types of inductors and various potting compounds were investigated. A discussion of this study is given in Appendix B, Sections 3, 4, and 7, of this report. The coil selected was fabricated by loose winding #18 wire on a 1/2" Rexolite rod. It was mounted away from other components and the side plates of the chassis, and the entire assembly was potted in "Eccomold L65." Potting causes some difficulties, discussed in Appendix B, Section 8 of this report.

The VFO was tested by techniques described in Appendix B. The significant results of the test are as follows:

The oscillator tuning range is 17.8125 Mc to 28.750 Mc for a control voltage range of +3V to +120V. Oscillator short term stability when measured as described in Appendix B-3 and without the phase-lock loop is approximately ±1.75 ppm. Long term stability as indicated by graph, Figure 19, is 20 Kc per degree C.

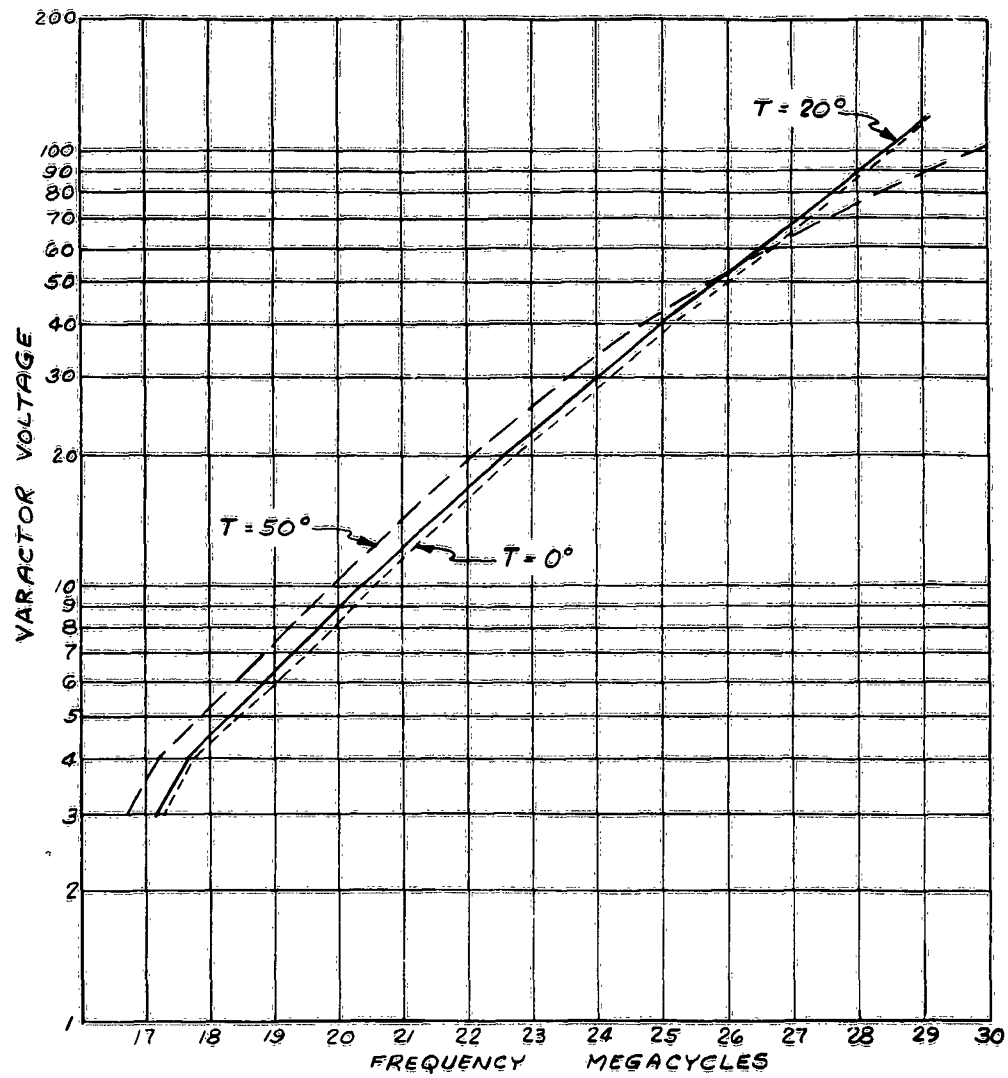


Figure 19. VFO Frequency vs Temperature

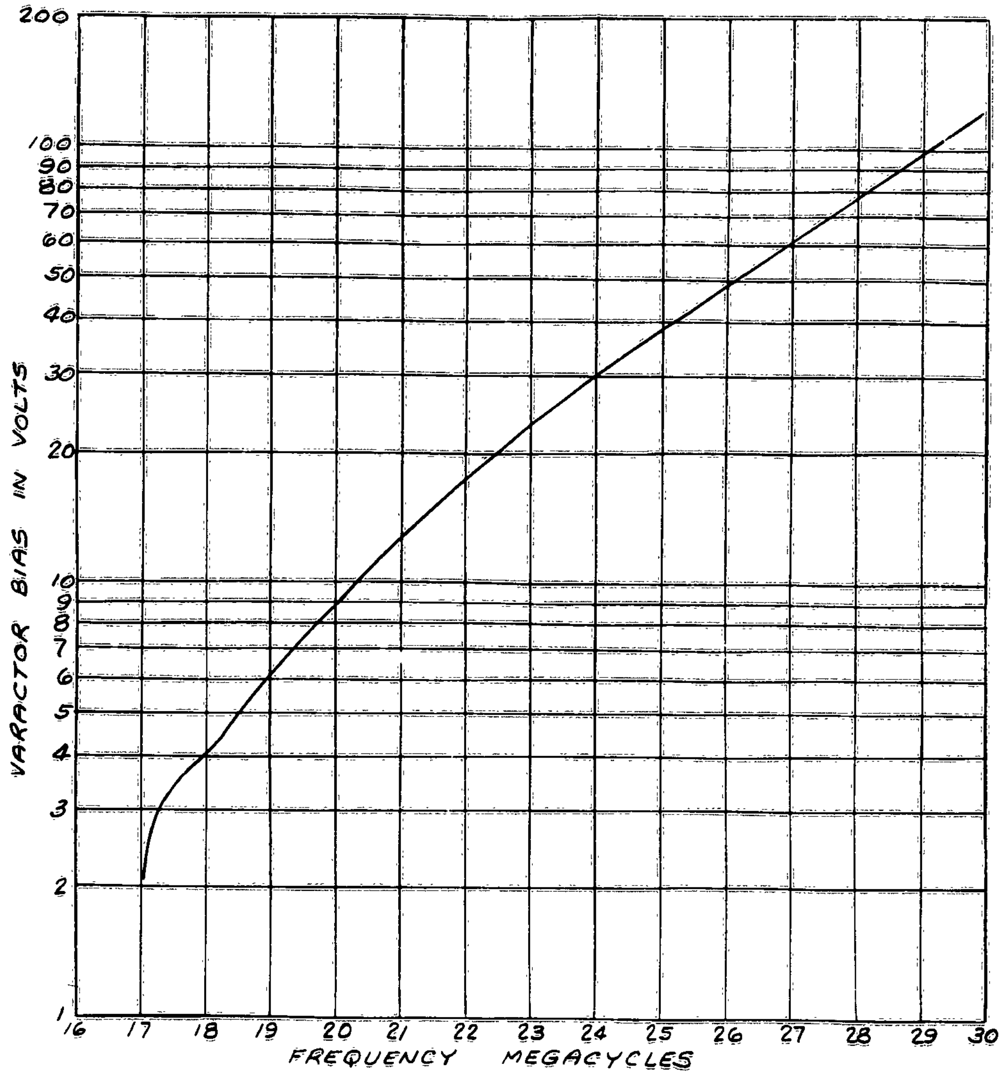


Figure 20. Varactor Bias vs Frequency

Both long and short term stability are improved when the oscillator is controlled by the phase locked loop. The long term stability becomes equal to that of the crystal reference oscillator, whereas the short term stability is determined by both the short term stability of the crystal oscillator and the response of the phase locked loop. It was found in testing the VFO (refer to Appendix B) that the rate at which the majority of VFO frequency deviations occurred was less than 100 cps, a rate which falls within the control loop response.

The VFO stability was measured in the receiver, with the phase locked loop closed. Both long and short term stability were found to be equal to that of the crystal reference oscillator when measured by a frequency counter, (Hewlett Packard Model 524). The oscillator was tested at vibration frequencies of 60 to 1000 cps at 15 G's in all three planes. No significant changes in the performance of the oscillator were noted either during or following the vibration tests.

The VFO is constructed in three shielded compartments. The first compartment contains the frequency sensitive components of the oscillator circuit and the lead side of the transistor. The two tuning varactors are mounted above the coil with silver strap and brass ferrules to reduce lead inductance. The second shielded compartment contains the buffer amplifier stage Q2, and the third shielded compartment contains the power and control line filters.

4.4 HARMONIC GENERATOR

The harmonic generator hardware is divided into two units. The major portion is shown in Figure 21 and a block diagram is shown in Figure 22. It contains three amplifiers, an emitter follower and three frequency doublers. The other portion of the harmonic generator (a doubler) is located in the stripline RF front end section (reference Section 4.1).

The function of the composite harmonic generator is to deliver to the mixer one milliwatt of RF power at the 16th harmonic of the variable frequency oscillator.

The multiplication is accomplished using four transistor frequency doublers, tuned by varactors. Each frequency doubler is tuned with a steped preset voltage which corresponds to every 1-Mc change of the receiver frequency. The tuning curve for the harmonic generator is approximately a 4th order curve and is similar to the curve of Figure 20. This curve was obtained by monitoring the preset voltage required to tune the variable frequency oscillator to the center of the lock range of the phase lock loop (while operating). The harmonic generator tank circuit inductors were then adjusted so that the harmonic generator tuning curve tracked the VFO tuning curve. The resistors for the voltage divider, needed to approximate this tuning curve, were chosen to give the exact voltages at every 10-Mc position, i.e.: 230-Mc, 240-Mc. The units Mc voltages between any adjacent 10 Mc voltages on the curve were assumed to be linear.

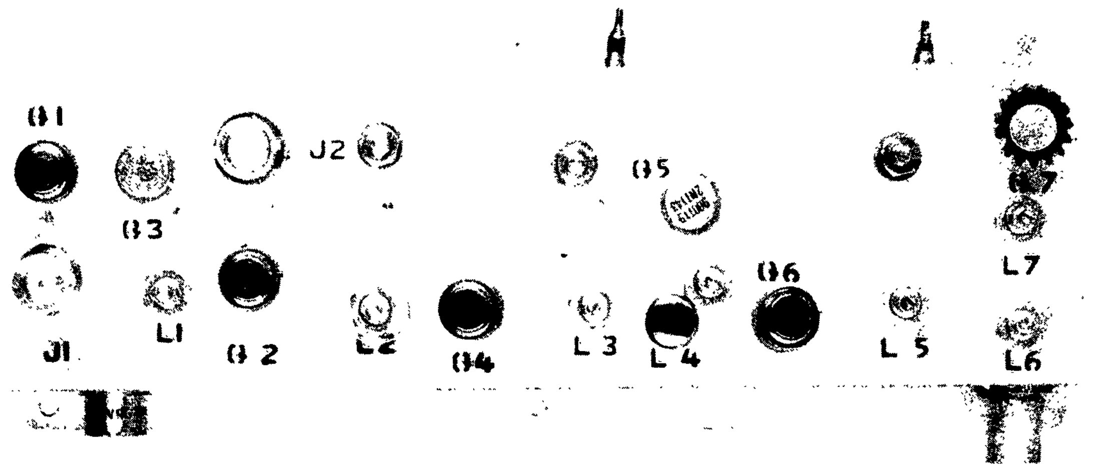


Figure 21. Harmonic Generator

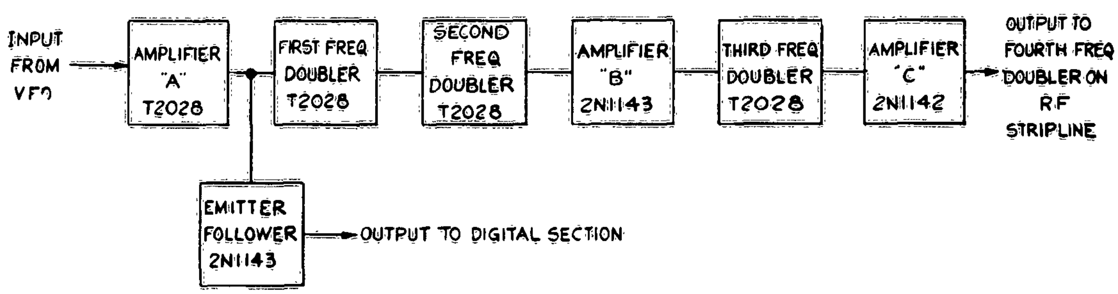


Figure 22. Harmonic Generator Block Diagram

Each frequency doubler has a 5.5 db loss. Therefore, the composite harmonic generator has a total loss of 22 db. (4 x 5.5). The variable frequency oscillator output is at -10 dbm. which means a gain of 32 db is needed to supply 1 milliwatt to the mixer. This gain is acquired with three wideband transistor amplifiers.

Referring to the schematic (Figure 23), the harmonic generator operates as follows: The first amplifier, Q1, receives a signal (17.8125-Mc to 28.74375 Mc) from the variable frequency oscillator and amplifies it to drive the first frequency doubler, Q2, and an emitter follower, Q3. The emitter follower supplies the digital phase lock section with the variable frequency oscillator output. The emitter follower is used to obtain loading isolation and drive into the digital section. The first amplifier has a gain of 13 db over the desired frequency range. The first doubler, Q2, is operated class C and is tuned by the varactor, CR1, to a frequency which is twice the input frequency. The resistor, R, is used to lower the Q of the tank circuit to alleviate the problem of the signal being larger than the bias voltage on the varactor. When the signal is larger it is rectified by the varactor and is added to the bias, this changes the capacitance of the varactor thereby changing the resonance point. It is advisable to do any multiplying at low signal levels, and then amplify if the frequencies are in a range where amplification is feasible.

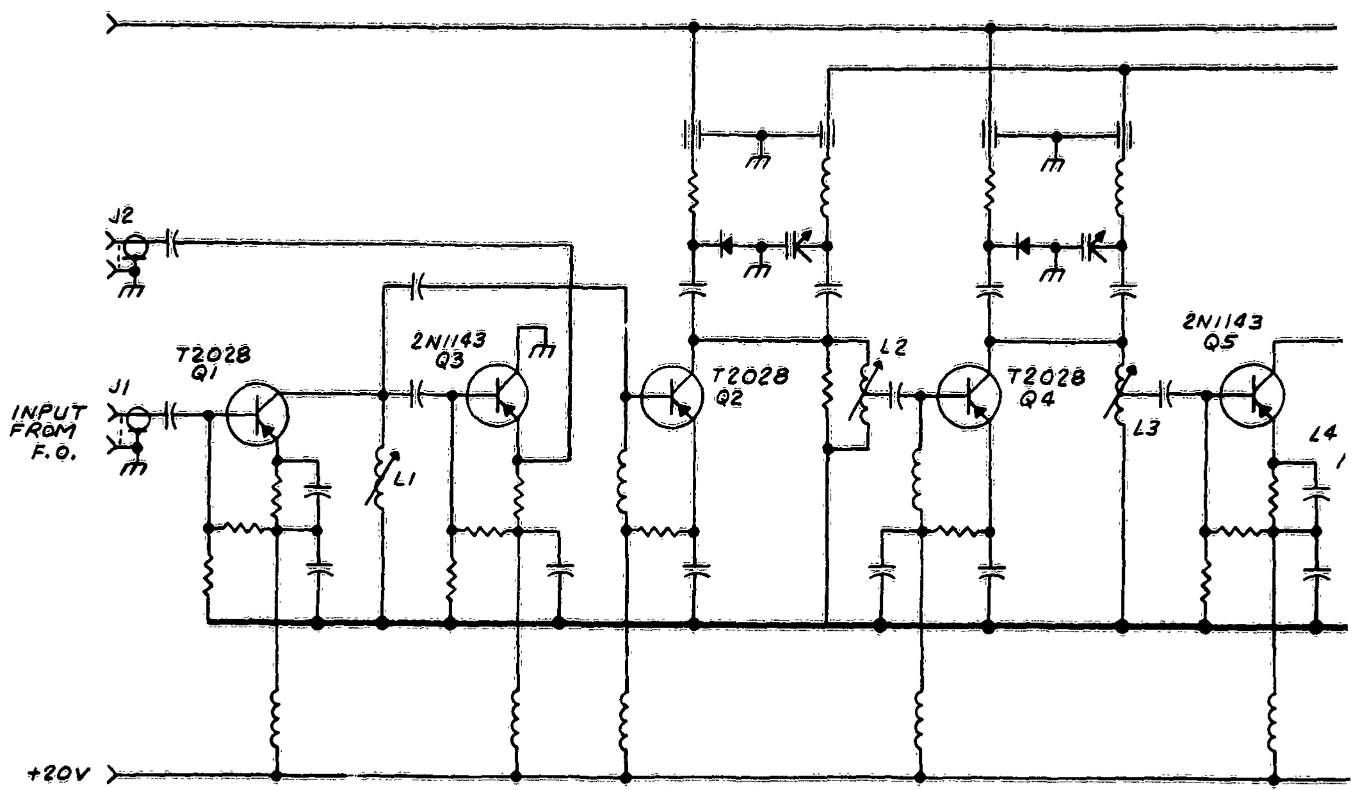
The first doubler, Q2, is biased class "C" and drives the second doubler, Q4, which again doubles the frequency with a class C (varactor tuned) circuit. The second amplifier, Q5, is fed from the second doubler and is a class A amplifier utilizing single tuned circuits. It has a gain of 13 db over the frequency range of 71.25-Mc to 115-Mc with the broad band amplifier tuned at 100-Mc. This amplifier drives the third doubler, Q6, which is again a class C operated T2028 transistor with a varactor tuned output circuit driving, Q7, the third amplifier. This amplifier is a double tuned Class A amplifier with a gain of 7 db over the frequency range of 142.5-Mc to 230-Mc.

The fourth frequency doubler circuit is identical to the first three doublers but due to the frequencies involved, 285-Mc to 460-Mc, it was built on the stripline with the RF front end and mixer. (Reference paragraph 4.1)

The three doublers each have a detector placed on the tank circuit alignment. This tuning device which remains on the tuned circuit at all times precludes the frequency shift or misalignment which takes place when an AC probe of a VTVM is connected and disconnected to the circuit involved.

The +20 volt line to each circuit and the tuning control line to each varactor is decoupled by an L-C section of sufficient values to keep any RF signals off these dc voltage lines.

11


J2
T2028
Q1
2N1143
Q3
T2028
Q2
L2
T2028
Q4
2N1143
Q5
J1
INPUT
FROM
F.O.
L1
L3
L4
+20V

Fig

2

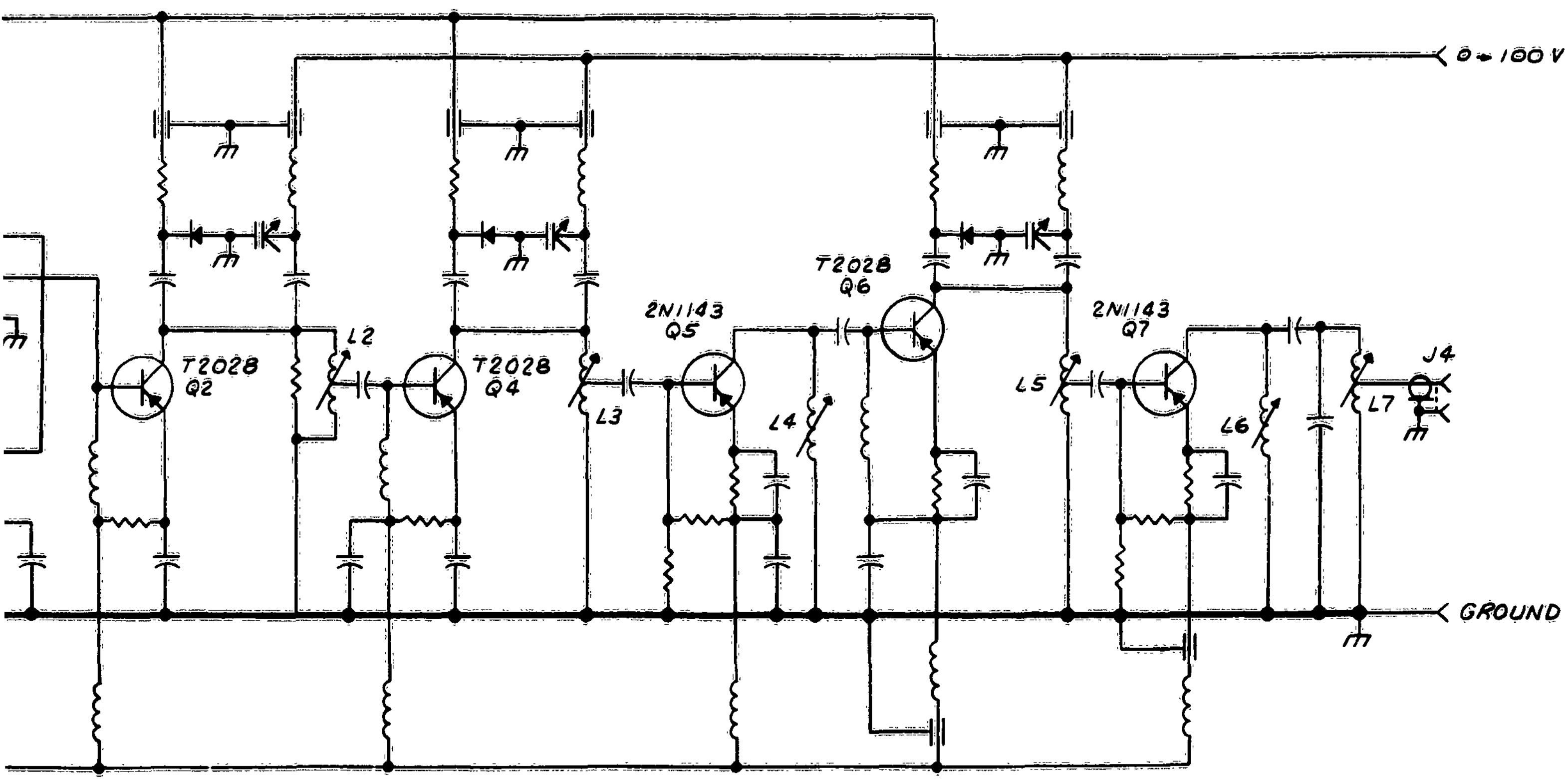


Figure 23. Harmonic Generator Schematic Diagram

5. ANCILLARY EQUIPMENT

Section 5 contains a description of the ancillary units of the UHF Solid State Tuning Device. The units in this category are those that are fixed tuned or those that are not directly connected with the channelling mechanism.

5.1 SECOND MIXER

The second mixer is illustrated in pictorial Figure 24, and a block diagram of this unit is shown in Figure 25. The function of this assembly is to amplify the 60 Mc signals from the first mixer (located in the front end assembly), convert them to a 10.7 Mc IF frequency, and provide the necessary image rejection and noise figure at the input terminals. This unit also contains the crystal filter selectivity package for 100Kc channel spacing in the receiver.

Theory of Operation:

Refer to schematic diagram, Figure 26.

Signals from the first mixer are amplified by the first stage, Q1. The gain of this amplifier is controlled by the AGC line to prevent overdriving at high signal levels. The tuned circuit containing C1 and L1 is resonant at 60 Mc to improve the image rejection of the second mixer. Local oscillator drive for the mixer is produced by oscillator Q2, which operates at a crystal controlled frequency of 49.3 Mc. The 60 Mc signal and the 49.3 Mc oscillator signal are combined in mixer Q3 to produce an IF frequency of 10.7 Mc. The mixer output is fed through crystal filter FL1 which provides the proper bandpass for 100Kc channel spacing.

5.2 IF AMPLIFIER

The IF amplifier is shown in pictorial Figure 27. A block diagram of the IF amplifier is shown in Figure 28. The IF amplifier produces approximately 85 db of gain at 10.7 Mc. The audio portion of the signal is detected and amplified to provide 50 milliwatts of audio output. An AGC detector and amplifier are also provided to develop a gain control voltage for the first three 10.7 Mc amplifier stages, the 60 Mc amplifier in the 2nd mixer assembly, and the RF amplifier stages in the front-end assembly.

A schematic diagram of the IF amplifier is shown in Figure 29.

5.3 REFERENCE GENERATOR

The reference generator shown in Figure 30 supplies the accurate clock pulse to the digital synthesizer for its use as a reference in maintaining accurate frequency.

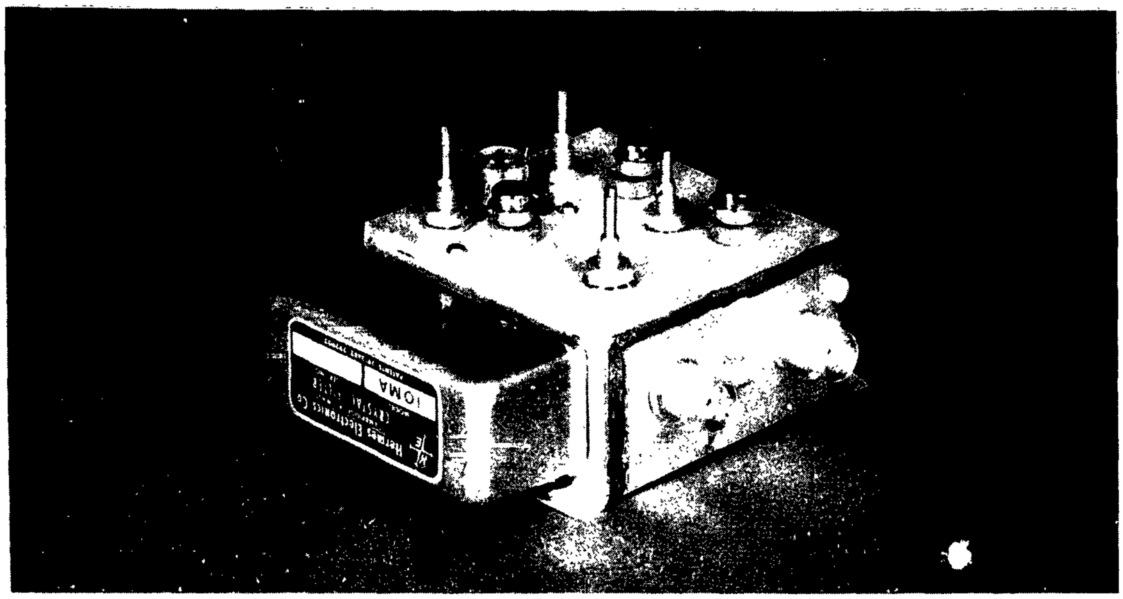


Figure 24. Second Mixer Unit

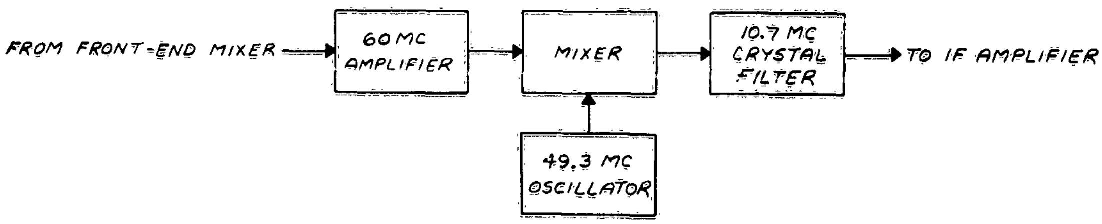


Figure 25. Second Mixer Block Diagram

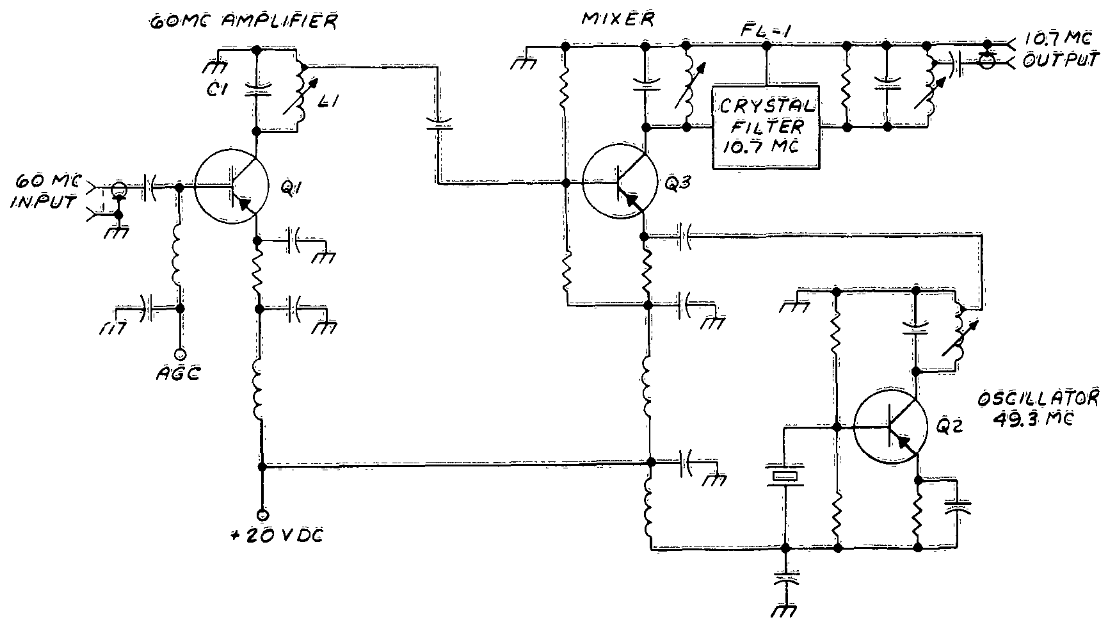


Figure 26. Second Mixer Schematic Diagram

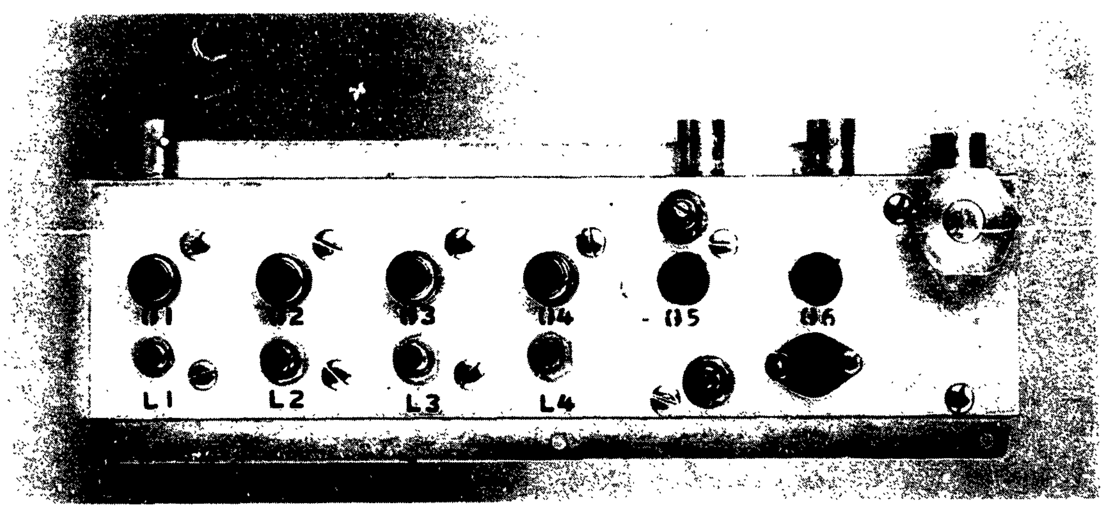


Figure 27. IF Amplifier

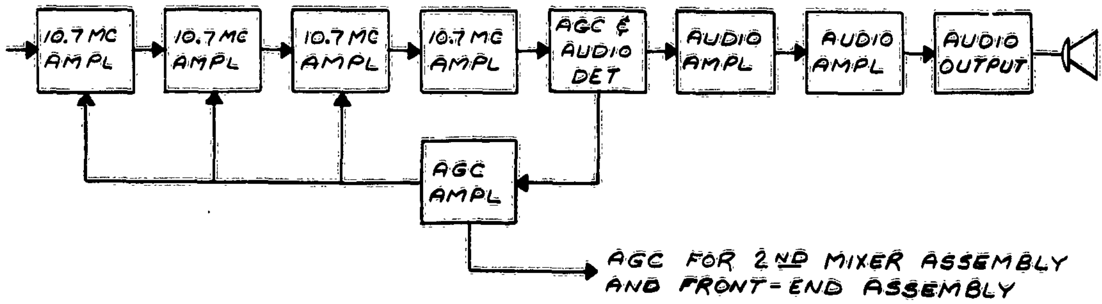


Figure 28. IF Amplifier Block Diagram

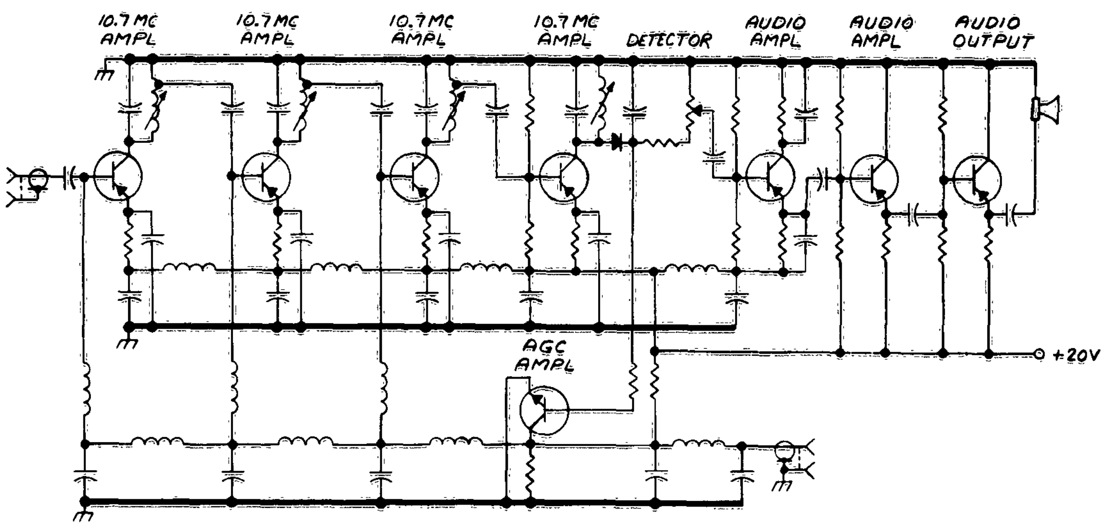


Figure 29. IF Amplifier Schematic Diagram

Figure 30. Reference Oscillator

The 100 Kc reference oscillator (see schematic, Figure 31) is a crystal controlled oscillator using a 2N332 silicon transistor, Q_1. The crystal unit is placed in series with the feedback connection from the capacitively-tapped tuned collector circuit to the emitter. The use of a tuned collector circuit prevents oscillation at spurious crystal frequencies. The oscillator output is fed into the amplifier clipper Q_2, through capacitor C_6. This amplifier is overdriven to give a 1 microsecond rise time, 6 volt peak-peak square wave output to drive the divide by sixteen digital circuitry.

The oscillator and amplifier-clipper were tested for frequency stability for variations of temperature and supply voltage. For a supply voltage variation of ±10 percent, the frequency variation was less than .1 cycle. A temperature variation of 50°C (0° to 50°C) produced a frequency variation of 3.8 cycles. This frequency variation is caused by the crystal unit itself. This stability was acceptable for this model. If the crystal unit were placed in an oven a stability of one part in 10^6 could easily be obtained.

5.4 POWER SUPPLY

The power supply shown in pictorial Figure 32 is designed to operate on 115 Volts, 60 cps. There are four outputs available; +6 volts at 1 ampere, -6 volts at 100 milliampere, +20 volts at 120 milliamperes and 120 volts at 15 milliamperes. The supply was designed to meet the following specifications:

> +6 volt, -6 volt and +20 volt outputs: ±5 percent regulation for ±10 percent line variations, ±10 percent load variations and temperature range 0°C to 50°C. Ripple 10 millivolts.
>
> 120 volt output: ±1 percent regulation for ±10 percent line variations, ±10 percent load variations and temperature range 0°C to 50°C. Ripple 1 millivolt and all outputs adjustable ±5 percent.

Refer to schematic Figure 33. The transformer, T1, supplies four series transistor regulators through four center-tapped secondaries. The secondary voltages are full wave rectified, and filtered by capacitor input filters.

The +20 volt regulator uses a single transistor, Q1, as a series regulator. The zener diode, CR9, is used for a reference with the potentiometer, R3, providing output voltage variation by tapping down from the zener reference voltage. Resistor R2 provides current to keep the zener diode CR9 conducting. Capacitor C2 is used for ripple reduction, with its capacity being multiplied by the dc beta of transistor Q1 and effectively placed across the output terminals. Resistor R1 is used to reduce the input voltage to the regulator which was somewhat higher than necessary from the transformer. Regulation is obtained as follows: if the output voltage increases the base-emitter voltage of A1 decreases causing its impedance to increase which decreases the output voltage. If the output voltage decreases, the impedance of Q1 decreases causing the output voltage to increase.

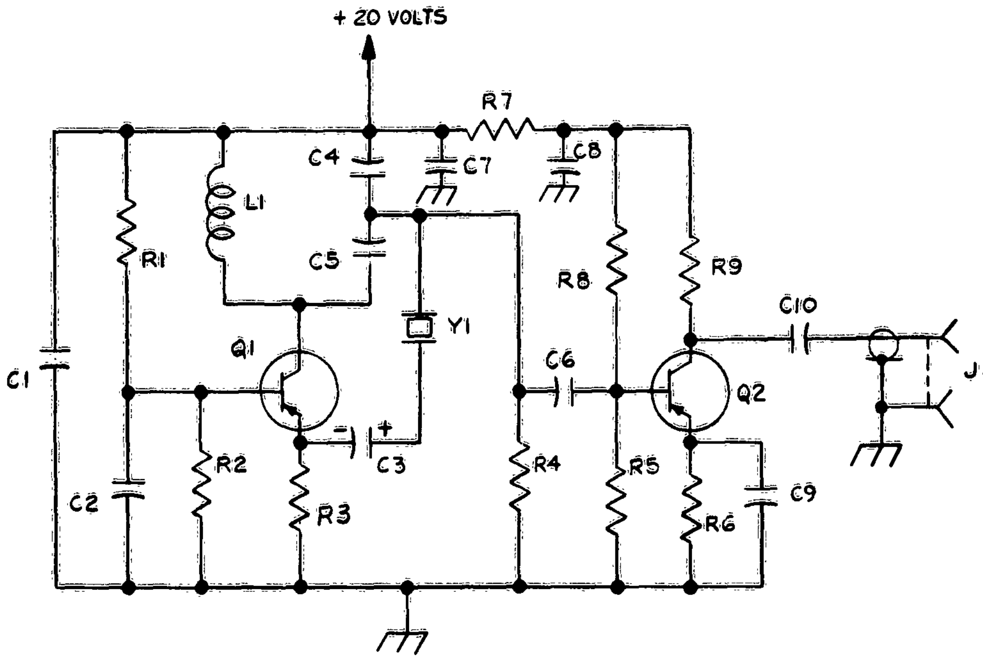


Figure 31. Reference Oscillator Schematic Diagram

Figure 32. Power Supply

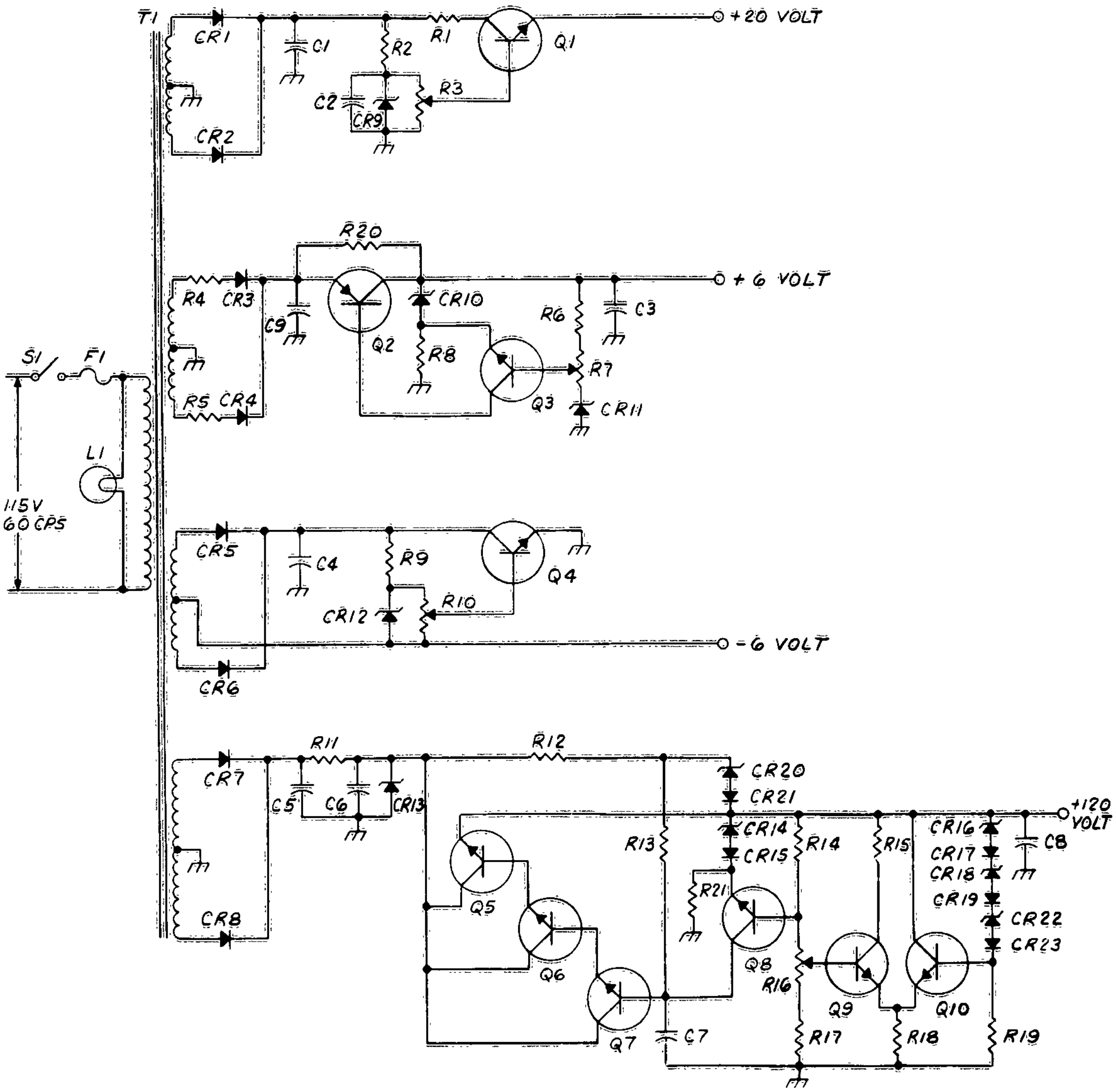


Figure 33. Power Supply Schematic Diagram

The +6 volt regulator uses a series transistor, Q2, driven by the comparator amplifier Q3. The zener diode CR11 sets a reference voltage which is adjustable for output voltage adjustments through potentiometer R7. The zener diode CR10 senses errors in the output voltage. The current to CR10 is supplied by resistor R8, while resistors R6 and R7 supply current to CR11. The regulator operates as follows; if the output voltage decreases, the base-emitter voltage of Q3 increases causing Q3 to conduct harder which causes Q2 to be turned on, thereby decreasing its series impedance and increasing the output voltage. Conversely if the output voltage should increase, transistor Q3 will be turned off causing the impedance of Q2 to increase and therefore decreasing the output voltage. The resistor R20 assures turn on of the regulator at low temperature. Capacitor C3 is used for ripple reduction.

The -6 volt regulator is a single transistor regulator using the zener diode CR12 as a reference. Potentiometer R10 provides for output voltage adjustment. Resistor R9 maintains the proper current to the zener diode CR12. Operation of the regulator is identical to the +20 volt regulator.

The +120 volt regulator is preregulated by the zener diode CR13 to compensate for input voltage variations. The transistors Q9 and Q10 form a differential amplifier. The base of Q10 is referred to the plus terminal of the regulated output with three zener diodes such that its potential is maintained at a constant voltage (approx. 15 V) below that of the output terminal. The base of Q9 is connected to a tap on the bleeder across the regulator output. Since the emitters of Q9 and Q10 are common, regulator action is such to maintain zero potential difference between their bases. Therefore, the output voltage will be that required to maintain the bleeder current at a value that will keep the potential between the regulated output and the base of Q9 at the constant zener voltage (15V). Error signals appear between the base of Q9 and Q10 and are amplified by Q9 and Q8. The current gain necessary to supply the drive requirements of the series regulator, Q5, is provided by Q7 and Q6. The emitter of Q8 is decoupled and bypassed by CR14 a reference diode. The collector supply voltage of Q8 is decoupled and bypassed by an additional zener diode, CR20. The action of this diode is such to prevent the injection of input voltage variations into the regulator amplifier. The stabistors CR17, CR19, CR21 and CR23 are used for temperature compensation of the zener diodes. The potentiometer, R16, in the base bleeder of Q9 provides output voltage adjustment. The capacitor, C7, reduces the gain at high frequencies and thereby provides the necessary phase margin to prevent oscillations.

The operating characteristics of the regulators are tabulated below:

Parameter	Regulator Output			
	+6 volt	-6 volt	+20 volt	+120 volt
Output voltage	6.0 to 9.6V	0 to 7.2V	0 to 22.5V	115 to 150V
Output load current	1.2 amp	130 ma	140 ma	15 ma
Ambient temp. range	0° to 50°C	0° to 50°C	0° to 50°C	0° to 50°C
Output Ripple	< 5 mv	< 10 mv	< 12 mv	< 1 mv
Load Regulation (±10% load variation)	1%	1%	1%	5 mv change
Line Regulation (±10% input voltage variation)	1%	1%	1%	5 mv change

The physical size of the power supply unit is 15 inches wide by 8 inches high by 8 inches deep. The unit weight 13 pounds.

5.5 FREQUENCY CONTROL

The voltage required to tune the front end is obtained from a voltage divider composed of precision wire-wound resistors which supply the 10 Mc steps and standard composition resistors which supply the 1 Mc steps. (Reference Figure 34.) Tuning data indicates that the precision resistors must be of ±.5 percent tolerance, whereas the composition resistors may have ±5% tolerance. Examination of the tuning curves shown in Figure 13 (B) will show that the voltage steps over any 10 Mc interval in the band can be supplied by this linear divider, while the 10 Mc steps must be obtained from the precision nonlinear divider.

Frequency Selector Switches:

The frequency selector switches perform two main functions in tuning the receiver:

a. They provide all of the varactor control voltages necessary for tuning (a) front end (b) harmonic generator (c) VFO.

b. They perform the necessary switching in the digital circuitry to allow phase locking of the VFO for 100 Kc channel spacing.

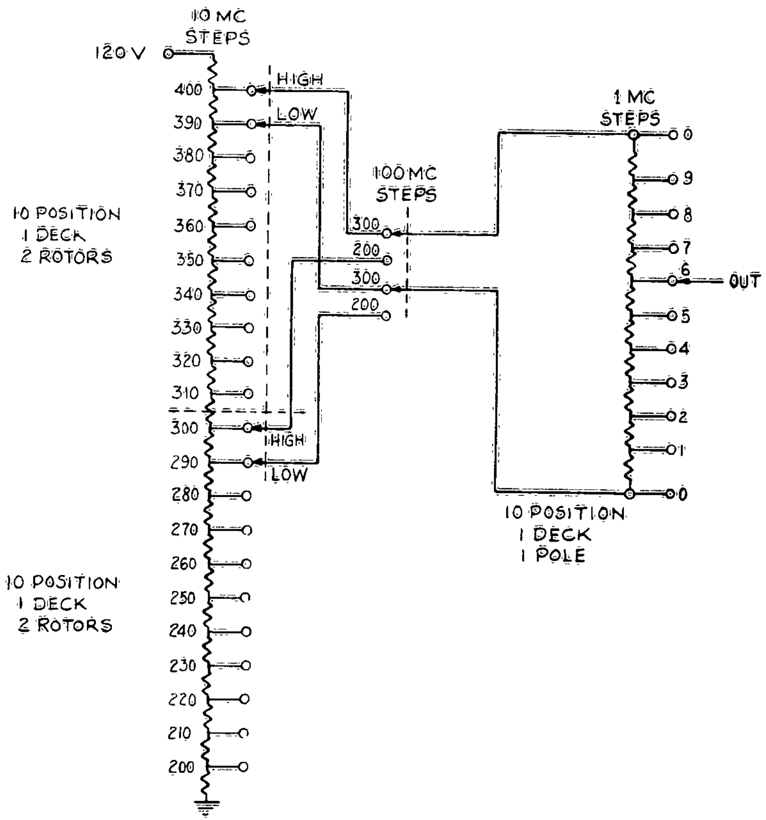


Figure 34. Tuner Decode Schematic Diagram

6. CONCLUSION

The design and construction of a solid state tuning device such as the unit reported herein is entirely feasible and such a system can be made to pass rigid environmental specifications by incorporating some design modifications. The most serious environmental condition is that of temperature variations. Inductances can be made reasonably stable. However, varactors and transistors change capacitance rather violently with change in ambient temperature. This change in capacitance can be predicted, and remains the same for thousands of temperature cycles. Considering the present "state of the art" of varactor diodes and the limitations on their useable capacity swing, temperature compensation by the use of fixed temperature compensating capacitors would seriously limit the tuning band of the receiver. Temperature conpensation should be accomplished by changing the operating point of the DC control line. Temperature compensation in the capacitive elements will require the use of diode band switching of inductances in that present day diodes (TYPICAL OF MA 4358F) barely have sufficient change in capacity to allow the tuning of the band from 225 to 400 Mc.

Other environmental conditions (humidity, salt spray, altitude, shock and vibration, dust, etc.) can be controlled by the use of incapsulation of sub units.

During the construction of the hardware, the varactors were interchanged with each other and no tracking problems were encountered. However, only a limited number (4) were interchanged and all of these can be assumed to be from the same production batch. A more representative general production quantity should be checked prior to drawing any firm interchangeability conclusion.

The solid state tuning device tunes so rapidly that it can be considered instantaneous, (approximately 10 milliseconds). This extremely rapid tuning of the multi channel device (as is) may have some serious human factor drawbacks. If one considers the sudden interruption of a train of thought from a burst of irrelevant communications or signal while the pilot is trying to remember a four digit channel number or any other memory requirement; some degree of confusion could be experienced. This type of interruption can be experienced while the pilot is tuning the receiver, if prior to the selection of the last digit of the desired channel, an operating channel is tuned in.

One solution to this problem would be to devise a sensing device which disables the audio until the fourth or last digit is selected, and if the fourth digit is not selected in a prescribed length of time the audio is automatically enabled.

APPENDIX A

DESIGN CONSIDERATIONS OF THE RF AMPLIFIER

1. INTRODUCTION

Section 1 contains a discussion of various design consideration of the RF amplifier. The following subjects are treated:

a. Proper placement of the RF band pass circuitry.

b. Diode switching of the tank circuits.

c. Voltage variable inductances vs voltage variable capacitor.

d. Characteristics of diode mixers vs transistor mixers.

2. RF AMPLIFIER

Figures 35 and 36 show two possible circuit configurations that can be used to provide the desired characteristics of the RF amplifier section. The circuit configuration shown in Figure 36 was selected as the basis for design in this receiver for the following reasons.

a. In the wide band amplifier, scheme shown in Figure 35, the amplifier must necessarily be placed ahead of the filter to provide the desired noise figure. The filter cannot be placed ahead of the amplifier since its insertion loss would contribute directly to the receive noise figure. A lossless filter would obviously be satisfactory in this arrangement, but such a filter cannot be constructed without losses in this band of frequencies. The tuning of the filter would be best accomplished by using voltage variable capacity diodes. To tune this range of frequencies (225 to 400 Mc) the Q of these diodes is not sufficient to prevent losses, therefore the losses of the filter could not be kept low enough to prevent degradation of the noise figure. Hence, the amplifier would need to be placed ahead of the filter. However, this arrangement is also unsatisfactory since it produces the same amount of amplification for undesirable signals within the 225 to 400 Mc band as it does for the desired signal.

In comparison, the circuit configuration shown in Figure 36 does not exhibit either of the disadvantages of the wide band

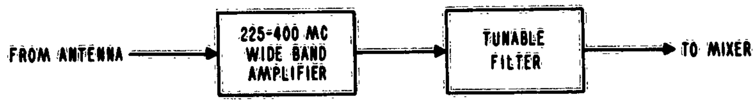


Figure 35. Possible RF Amplifier Section Block Diagram

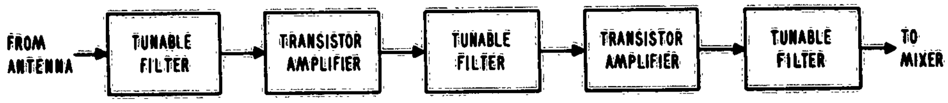


Figure 36. 225 to 400-MC RF Amplifier Section Block Diagram

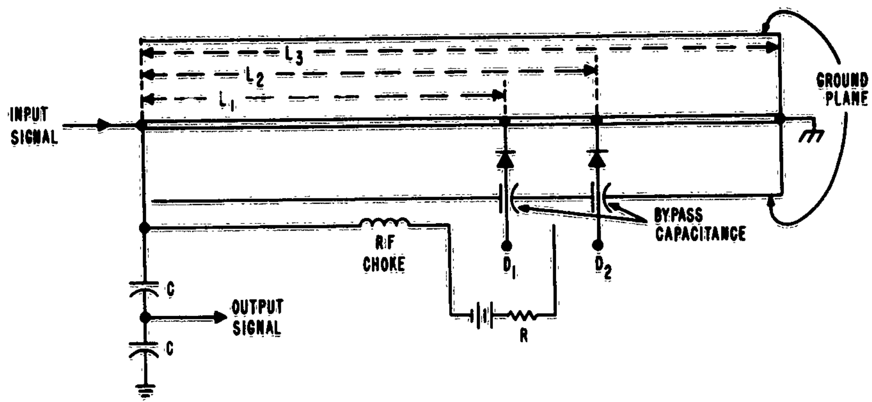


Figure 37. Variable Length Transmission Line Tuned Circuit

scheme, while it does contribute some advantages of its own. The single tuned circuit shown at the input can be constructed so as to present an impedance match for the antenna; provide some selectivity ahead of the first amplifier; yet at the same time, contribute very little to the noise figure of the receiver. The remaining tuned amplifier stages each contribute to the selectivity of the receiver while producing sufficient gain to allow the noise figure of the receiver to be determined by the input transistor.

This type of front end offers the additional advantage of utilizing single tuned circuits to provide selectivity. Since the circuits are voltage tuned, it is advantageous to have them single tuned and isolated from each other by the amplifiers to prevent interaction and permit the use of tracking devices.

It was decided, therefore, that the circuit configuration shown in Figure 36 was better suited to fulfill the requirements of this particular system.

3. VARIABLE REACTANCE COMPONENTS

The major problem in the RF amplifier section is that of tuning the frequency selective circuits over the desired frequency range. Three methods applicable to electronic tuning are: (a) current variable inductances; (b) transmission lines shorted to the appropriate length by diodes; and (c) voltage variable diode capacitors.

Current variable inductances, (the first method), have high loss at the frequencies of interest and require proportionally large power for tuning. Inductive hysterisis also injects many problems in tracking. This type of component is therefore considred unsuitable.

Figure 37 illustrates a second method of producing a parallel resonant circuit where the resonant frequency depends on the length, L, of the transmission line. The circuit can be tuned to a given frequency by forward biasing the appropriate diode. This type of circuit would be tuned across the band in a number of steps, the number of steps being determined by the operating Q of the circuit and the allowable variation in gain over the frequency band. The Q of the resonant circuits produced by this method depends, in part, on the dynamic resistance (R) of the diode when it is forward biased. The dynamic resistance of a diode is given by $R = \frac{L}{Ki}$, where i is the diode current and K = 20 for silicon and 7.5 for germanium diodes. To realize values of Q comparable with those obtained in circuits emoloying variable capacity diodes, R should be about 1 ohm. For a silicon diode $i = \frac{L}{20(1)} = 50$ MA, the disadvantages of the shorted transmission line technique are the large current required to short the diode effectively and the switching circuitry required.

The third and most acceptable method of tuning is by the use of variable capacity diodes.

Variable capacity diodes can be used in either lumped parameter or strip transmission line circuits to produce the desired tuned circuits. Strip transmission line offers some advantage in keeping the stray inductance and capacitance to a minimum.

Furthermore, they offer the advantage of reducing interstage coupling since the inductances in the resonant circuit can be closely situated and yet have little mutual coupling.

The previously mentioned advantages of the stripline can be noted in the photograph of the stripline assembly, Figure 10, which is found in Section 4. A more detailed description of the circuit is given in the theory of operation, paragraph 4.1.

4. MIXER

Investigation of mixers at 225 to 400 Mc reveals two applicable types, namely, a crystal or diode mixer, and a transistor mixer. The most appropriate type for the present application can be determined from consideration of the conversion gain, the frequency response, and the realizable noise figure of each type. Relative characteristics of diode mixers can be found by considering a circuit employing a good available diode, a 1N21F. The frequency response of this diode is reasonably flat over the range of interest and the conversion gain is about -4 db. The noise figure at the input to the mixer is given by

$$N_D = L_C (N_R + N_{IF} - 1)$$

where N_D = overall noise figure of mixer and IF (power ratio)

L_C = diode conversion loss (power ratio)

N_R = diode noise temperature (power ratio)

N_{IF} = IF amplifier noise figure (power ratio).

Assuming a 5 db noise figure for the IF amplifier and the parameters of the 1N21F diode,

$$N_D = 8.1 \text{ power ratio or } 9.1 \text{ db.}$$

Transistors mixers have a response which drops about 6 db from 225 to 400 Mc. Typical mixers employing T2029 transistors have noise figures of 7.5 db and a conversion gain of 16 db at 225 Mc. At 400 Mc, typical noise figures are 9 db and conversion gains are 10 db. The noise figure at the input to the transistor mixer is given by

$$N_T = F_M + \frac{F_{IF} - 1}{G_M}$$

where N_T = overall noise figure

F_M = noise figure of mixer

F_{IF} = noise figure of IF

G_M = conversion gain of mixer.

Assuming a 5db noise figure for the IF amplifier, $N_T = 7.6$ db at 225 Mc. At 400 Mc, $N_T = 9.1$ db. Comparing the diode and transistor mixer characteristics discussed above, it is evident that there is little difference in the noise figure at the input to the mixer for the two types. Thus the choice between the gain of the transistor mixer is not a handicap in the present application, and the transistor mixer is chosen because of the large conversion gain. Although gain is not of primary importance in the receiver used to demonstrate electronic tuning, the additional gain is desirable since it reduces the required IF gain. To realize this conversion gain, a local oscillator input power of about 1 milliwatt is required.

APPENDIX B

DESIGN CONSIDERATIONS OF THE VFO

APPENDIX B

DESIGN CONSIDERATION OF THE VFO

1. INTRODUCTION

Section 1 contains a discussion of the frequency stability of the VFO. Various means of obtaining frequency stability and techniques for measuring it are considered.

During the design phase of the program, it was decided that the response of the control loop should be from 0 to 100 cps. All design and tests of the VFO were made under the assumption that such a response would be used; however, a later redesign of the phase detector raised and improved the loop frequency response.

2. TECHNIQUES FOR MEASURING STABILITY

Stability must be related to the probability that the VFO frequency deviation will not exceed the bandpass requirements of the AM system. In addition, the rate at which the frequency deviations occur is of interest since the frequency deviations at rates below 100 cps will be reduced by the action of the phase-locked loop. Thus, the problem of measuring the VFO stability is one of determining the frequency spectrum of the VFO. Direct measurement of this spectrum with a spectrum analyzer is difficult because the spectrum is extremely narrow. An approximation to the VFO frequency spectrum can be obtained by mixing the oscillator signal with some reference to obtain a frequency in the neighborhood of 1 Kc, and then measuring the phase variations of this signal. To obtain a stable reference and to test the measuring technique, two 20-Mc crystal controlled oscillators were built. The output of each oscillator is fed into a transistor mixer. By pulling one of the oscillators with a shunt capacity, a beat frequency of 1 Kc is obtained. The 1-Kc signal is amplified and clipped, and applied to the vertical axis of a Tektronics 535A oscilloscope. A portion of the same signal is passed through a variable delay and used to trigger the sweep of the oscilloscope. Phase variations in the 1-Kc signal produce a jitter in the zero crossing as shown in Figure 38. Assuming that the frequency spectrum of the oscillators has a gaussian distribution, the phase jitter of 1-Kc signal can be converted to the oscillator frequency spectrum. The jitter of the 1-Kc signal is taken to be the distance from A to C as shown in the figure, where 9 out of 10 zero crossings occur.

This criterion corresponds to the 1.65 sigma values of the gaussian distribution. Figure 39 shows the frequency spectrum of the two crystal oscillators determined by this method. As stated earlier, this is an approximation

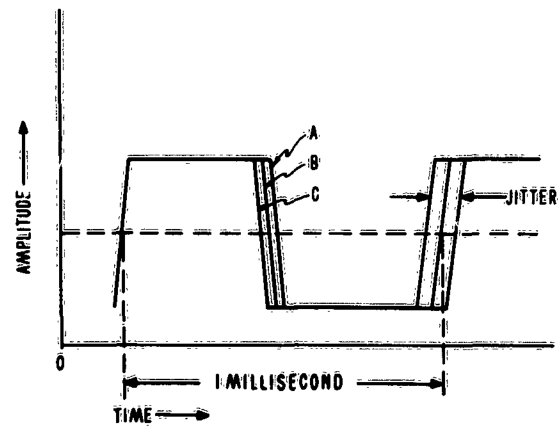


Figure 38. 1-KC Sine Wave After Clipping and Amplifying (as seen on scope)

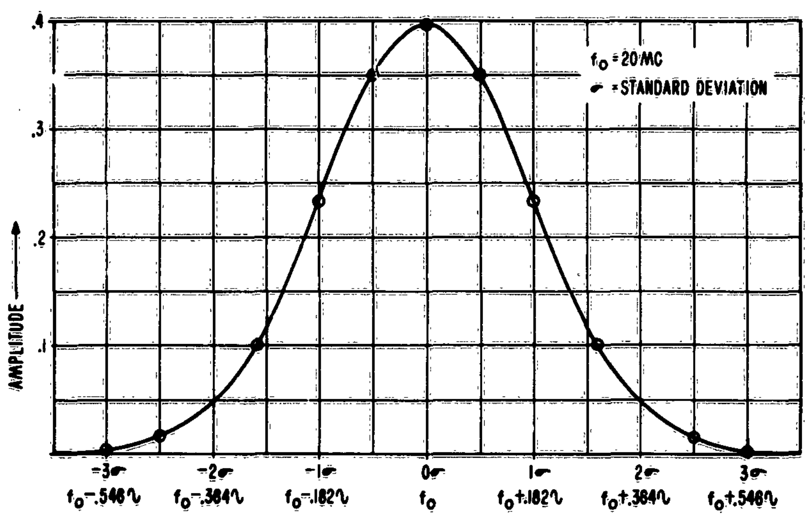


Figure 39. Crystal Oscillator Frequency Spectrum

to the frequency spectrum since the distribution is assumed and the interpretation of the criterion established depends on the judgement of an observer.

Tests were run on two crystal oscillators, effectively isolated and shielded from distributing infulences. By measuring the peak-to-peak jitter of the 1-Kc signal, it was found that the crystal oscillators were stable to about 3 parts in 10^8 over time periods varying from 1 millisecond (see Figure 40). This means that one oscillator is stable to about .707 x 3 parts in 10^8, or 2 parts in 10^8, which is adequate for use as the reference, against which to measure the VFO.

Actual measurements of VFO stability were made using the previously described method, substituting the VFO for one of the crystal oscillators. The jitter at a difference frequency of 1 Kc was then measured, and found to be approximately ±35 cps at the 20 Mc frequency. This represents a short term stability of 1.75 parts per million.

It was also desirable to determine the rate at which short term variations occur since this rate must fall within the control loop response of the VFO and phase lock system. To accomplish this measurement, the VFO and crystal oscillator were adjusted for a 1 Kc beat as described previously. Simultaneously the two signals were fed to a frequency discriminator, whose output was observed on a scope. The amplitude of the signal was a representation of the peak deviation of the VFO, while the frequency of the discriminator output signal was representative of the rate at which the deviation occurred. This rate was determined to be less than 100 cps, with the major portion of the variations occurring at 60 cps. The actual measurement of this rate was accomplished by the use of tunable electronic bandpass filters.

3. VFO INDUCTANCE

Consideration given to the selection of a proper induction for the VFO are listed in the following paragraph.

4. DEPOSITED COILS

Techniques have been developed for depositing coils in the form of square spirals on glass plates. The inductance of this type of coil is proportional to the length of line (assuming the width and thickness remain constant) and is about 25 nanohenries per inch. With the variable capacity diodes available today, an inductance of 1-5 microhenries is necessary to have the oscillator operate in the proper region. Assuming the worst case, i.e., 5 microhenries inductance, we see that this would take a line 200 inches long. Because of size restriction, the coil would have to be put on a plate, about two-by-two inches. To get this length of line on the plate, it would have to be a spiral whose line is

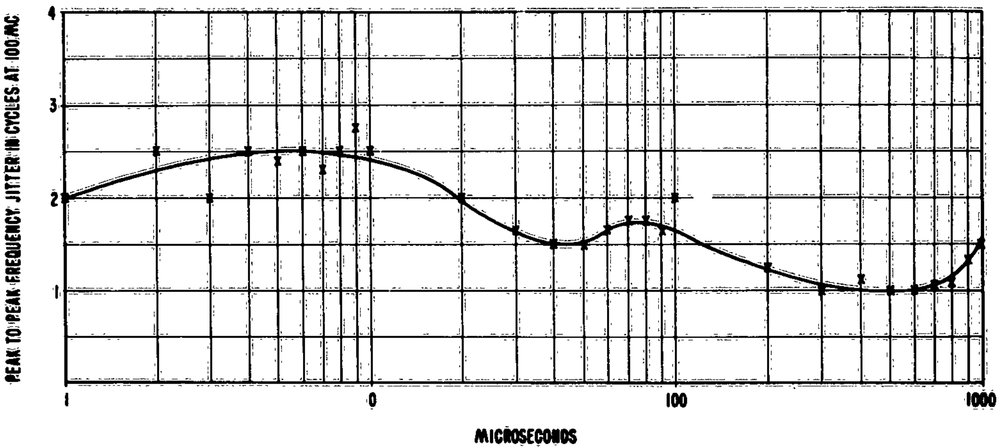


Figure 40. Data from Crystal Oscillators

10 mils wide, with a 5 mil spacing. Such a deposited metal line is so thin that it would have a resistance of approximately 20 ohms per inch. The Q of a coil of this type would be .16, which is much too low for this application.

5. ETCHED PRINTED CIRCUIT BOARDS

A coil having dimensions that are the same as the deposited coil described above and having a Q of 100 - 200 can be obtained by photo-etch techniques. The exact Q depends on the cross sectional area of the lines. This type etched coil has a usable Q, but since the stability of the oscillator is directly proportional to the Q, a coil of greater Q is desired.

6. TEFLON ROD

By pressing copper wire into groves cut in a Teflong rod 1/2-inch in diameter and 1-inch long, and spacing these groves 1/16 inch apart, an inductance of the proper value can be obtained. The Q of this coil is very high, but the mechanical stability of this coil is not as good as that of the etched circuit board.

7. POTTING COMPOUND

Several facts were considered in selecting a compound suitable for encapsulating the VFO components as discussed in the following paragraphs.

> The wide range of frequencies tuned by the VFO was difficult to obtain because of stray capacitance in the circuits. If the potting compound increased the stray capacitance, the tuning bandwidth would be decreased. It was therefore desirable to have a compound with a dielectric constant approaching that of air. A second consideration was that the oscillator was operating at low gain and with minimum drive. Hence, to prevent loss of drive, the compound must have a low dissipation factor. Actual values for the dielectric constant and dissipation factors that can be tolerated without destroying the properties of the VFO cannot be easily calculated, since the stray capacitance and drive level in the circuit cannot be measured accurately. Several glass-base compounds were investigated, but none exhibited the desirable properties. Materials such as teflon and polystyrene have the necessary electrical properties but they are not physically suited to potting.

The material selected for this particular application was a laminating resin "Eccomold L65." While it is actually intended for use as a laminating resin, it was felt that it might be suitable as a casting resin for the small volume required. The electrical properties of the material are particularly well suited. The dielectric constant is 2.55 at 10^8 to 10^{10} cps and the dissipation factor is .0004 to .0005 between 10^8 and 10^{10} cps respectively.

The entire oscillator buffer amplifier unit was filled with the compound, and the output of the circuit was monitored to determine the effects of the material upon oscillator stability and tuning range. At this point difficulty was encountered. The material failed to harden. It was felt that since the material was not specified to be used as a casting resin, it might require additional heat to activate the cure. The temperature was raised to 65°C for this purpose (65°C is below the maximum operating temperature of the transistor). As the material hardened, the oscillation ceased. The oscillator was made to operate again by removing most of the compound from the tank circuit elements, such that only the minimum amount required for mechanical support remained. Although the oscillations were strong again and the oscillator covered the desired tuning range, the frequency stability was degraded considerably. Replacing the transistor restored the circuit to proper operation.

Further investigation of the problems were not attempted since time did not permit. However, the following conclusions and recommendations are offered:

It may be concluded that (a) either the electrical properties of the compound changed during the curing process and thereby caused the circuit to fail; or (b) the exothermic temperature of the curing material raised the transistor temperature to a point where the transistor characteristics changed. It is recommended that a more extensive study of potting compounds (particularly the foamed type) should be made in an effort to avoid the problem. Manufacturer's data indicates that certain new types of foam materials may exhibit properties better suited to this application than the resin that was used.

APPENDIX C

DIGITAL SYNTHESIZER

APPENDIX C

DIGITAL SYNTHESIZER

Appendix C describes in detail, the configurations and operation of the circuits used in the digital portion of the frequency synthesizer. The basic digital building blocks are discussed followed by a description of each card. A fairly detailed discussion of the test procedures are given where critical performance areas or novel test methods warrant. A discussion is made of several performance deficiencies and their correction. Finally, the sampled phase detector is described.

Figure 15, in Section 4, shows a block diagram of the digital synthesizer system. By referring to this diagram, Appendix C can be more easily understood.

The entire device consists of a preset counter built on four plug-in cards, a fixed counter built on three plug-in cards, a pulse forming and control card, a scale-of-sixteen counter card and a phase detector card, making a total of ten cards.

The digital circuits were designed on a worst-case basis to insure satisfactory operation with plus-or-minus five percent voltage and resistor tolerances. Variation of loading conditions was taken into consideration.

The basic flip-flop shown in Figure 41 is essentially a circuit of the familiar configuration with additional diode gates at the transistor bases. The gate consisting of C_T, R_T, and the associated diode is the self-gated input. Complementing, or counting, is accomplished by tying the free ends of the C_T's together to form a single input. The time constant of this gate may be varied by changing R_T or C_T. This is of particular interest at lower speeds where R_T may be increased to reduce the loading on the previous circuit, thus increasing the fan-out ratio of the driving circuit. The next pair of gates are the preset gates, which consist of R_{PB}, R_{PC}, C_P, and the associated diodes. These gates are manually controlled by the frequency selector switches on the front panel. If R_{PC}, the preset control resistor is grounded through the switch, the gate is ON. The divider action of R_{PB} and R_{PC} maintains the cathode end of the diode slightly more positive than the base of an ON transistor. If the end of R_{PC} is left floating, the cathode of the diode is raised to the positive supply voltage which makes the gate inoperative. During presetting, a wide negative going pulse is applied to the capacitor inputs of both sides simultaneously. The switches are so arranged that one, and only one, gate on a givenflip-flop will pass the pulse. The preset gate is designed to pass a pulse into the base of sufficient width to override any tendency for the count to propagate from the previous stage. The overall effect is that the entire counter is forced to the desired state and held until all transients have ceased; then released.

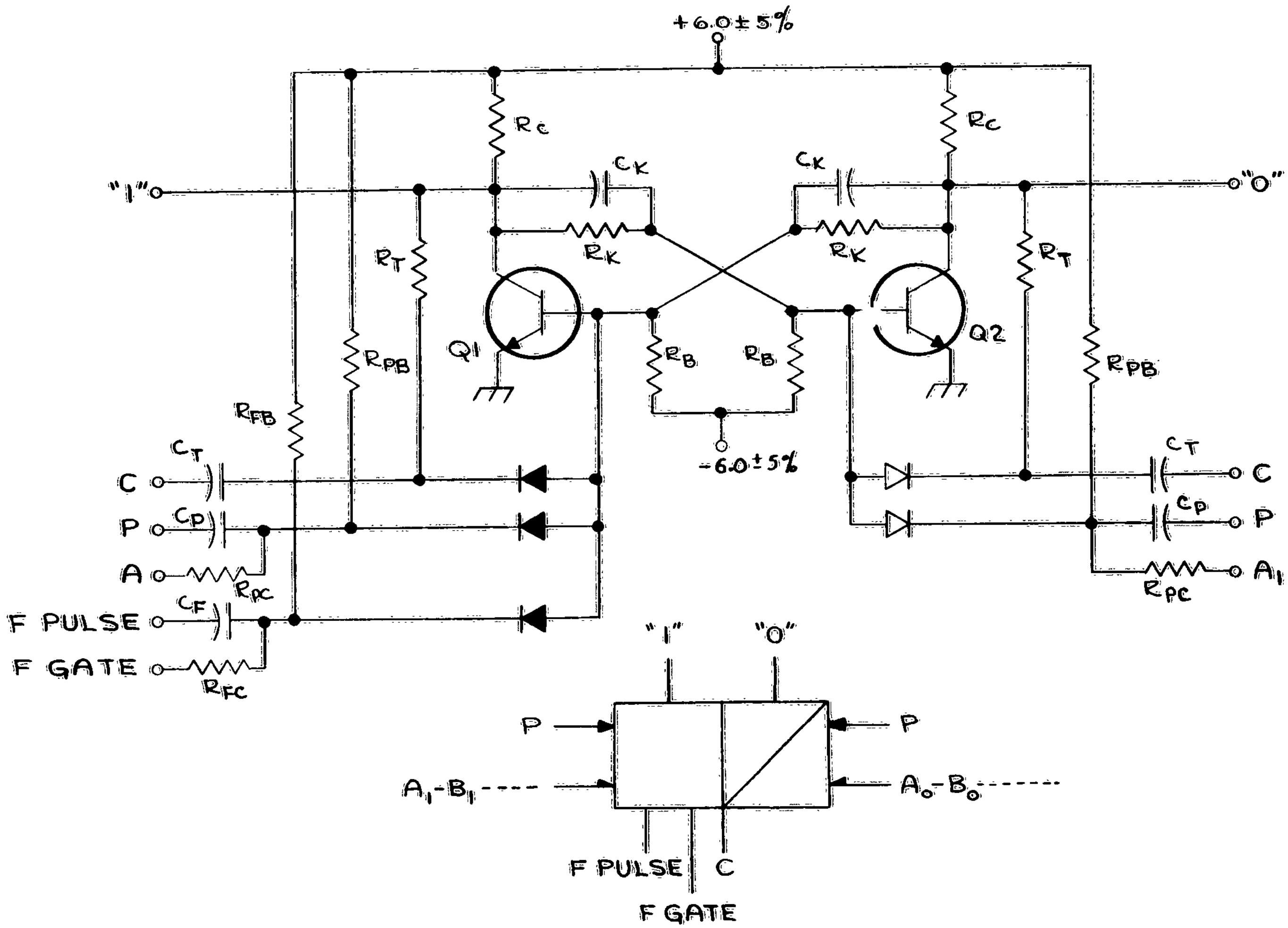


Figure 41. Basic Flip Flop

The remaining gate is the feed-back gate, consisting of R_{FB}, R_{FC}, C_F. It is shown on one side only, because the feed-back is always to one-side only. The basic operation is similar to the preset gates. It may be either controlled by the NOR in the feed back circuit, or R_{FC} may be gounded and the pulse actively gated.

It is here stated that in any application where any gate is not needed, it may be omitted in its entirety. It is also stated that due to the symmetrical nature of the circuit the feed-back gate could be on either side. Thus it may be implied that for a given application, any gate is used as needed; if the gate is not used, it is omitted, and a saving in cost and complexity is effected.

The basic NOR is shown in Figure 42. It accomplishes the familiar NOT-AND function to serve as a logic circuit, or as a gate. The resistor R1, R2, and R3 form a network to meet the necessary OFF and ON D.C. conditions. The capacitor C produces a high transient gain necessary for fast switching time. A great number of diodes may be used, the maximum is determined by the fact that diode leakage of the OFF diodes tend to increase the control current needed at the ON diodes. A lower practical limit cause by diode capacitance was found experimentally. A direct input may also be used where it is not advantageous to place the diodes physcially near the NOR. The 300 ohm collector resistor R_c is used to provide good fall times and prevent loss of signal amplitude when driving AC loads such as pulse inputs or gate resistors.

The single-shot shown in Figure 43, is used to generate a wide pulse, or to produce a delay in a switching transition. The direct coupled side is identical to that of the flip-flop. The "base-on" resistor, R_{BO}, is chosen to produce a stable ON condition in Q1. This in turn causes Q2 to be in a stable OFF condition. When a negative going transition occurs at the input end of C_T, Q1 is turned OFF which turns Q2 ON. The action of C_P drives the base of Q1 far negative for a time determined by the $R_{BO}\,C_P$ product. This transient is stopped at approximately half way with respect to voltage when Q1 again turns ON and restores the stable condition. The delay is approximately $0.7\,R_{BO}\,C_D$ seconds where R_{BO} and C_P are given in ohms and farads, respectively. Delay is adjusted by changing C_P rather than R_{BO} so as not to affect the D.C. stability. A recovery phase follows where C_D recharges through the collector resistor. The collector of Q1 produces a positive going rectangular pulse which is quite square. At the collector of Q2 a negative going pulse occurs with a trailing edge which is deteriorated due to the recovery phase.

The inverter-amplifier, shown in Figure 44, is used where isolation, greater driving capability, or inversion is desired along with no other logical function. It requires no diodes and fewer components than a NOR. The DC bias is similar to that of the NOR circuit. With the elimination of the diode, a resistor, corresponding to R_1 in the NOR circuit, may be combined to be a part of the collector resistor of the driving source. The other resistors,

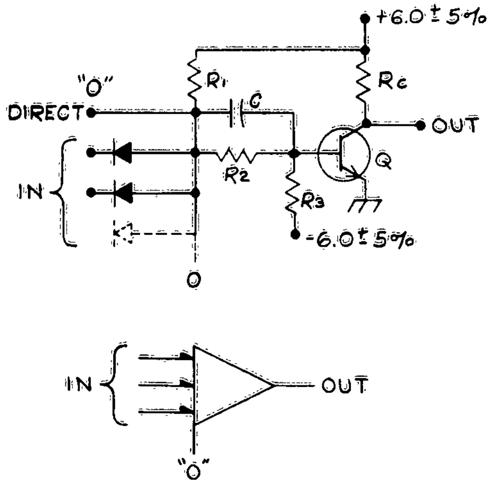


Figure 42. NOR (Gate)

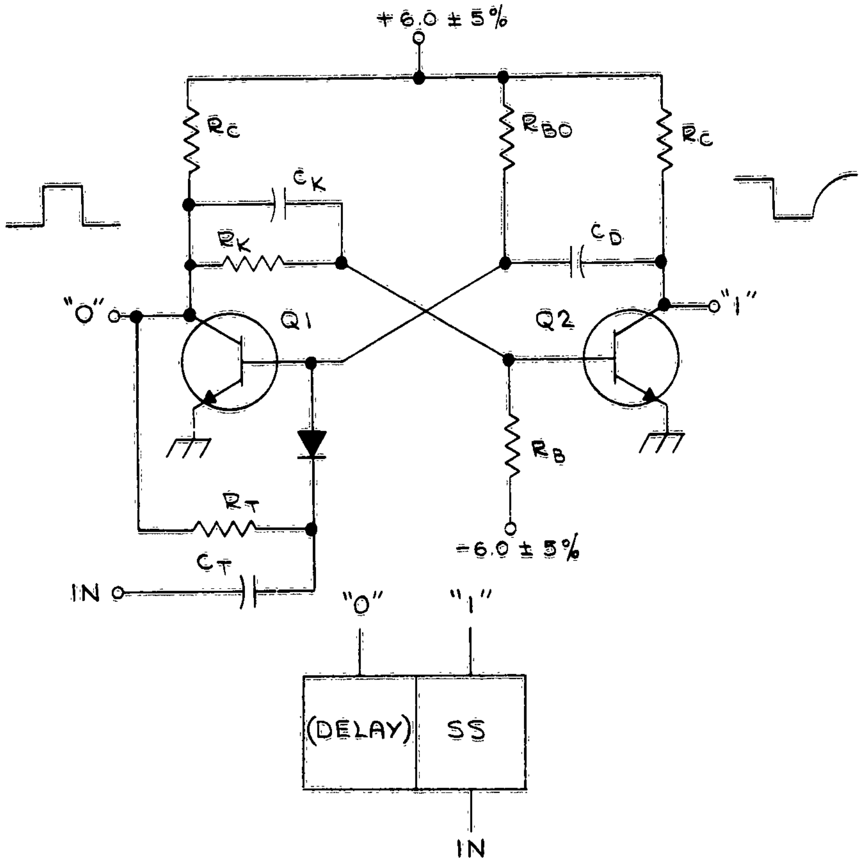


Figure 43. Single Shot

R_K and R_B, are now different from the corresponding resistors in the NOR circuit because the diode forward drop is eliminated. The capacitor C improves the transient gain; as in the NOR circuit. A fairly low value of R_C is used when driving AC loads for similar reasons as in the NOR circuit.

The broadband amplifier and pulse shaping circuits, shown in Figure 45, convert a low level sine wave to pulses. The output is very nearly independent of the input level above the minimum value of one volt peak to peak. The input could be padded with a shunt resistor to make the impedance 50 ohms. In this case, the input power required would be 2.5 milliwatts. It was felt that this was an unnecessary refinement, since the interconnecting cable will be very short. The actual input power from the VFO buffer is adequate as the circuit stands. The first two stages are broad-band amplifiers biased for small signal operation. The third stage is driven in a switched manner. The C-R-C tee section differentiates the resulting square wave to produce the pulse. Use of a tee section, instead of a simple RC, allows the differentiater time constant to be independent of the biasing resistor and permits a reasonable capacitor value which is large compared to stray capacitance. The last stage produces a logically inverted or $\bar{X}$ pulse which is needed at the counter gates and $\bar{X}$ input in the high-speed feed-back circuits. This method of pulse generation was used in preference to the usual Schmidt trigger and single-shot method, due to the difficulties caused by regeneration delay. In the system used here, slight propagation delays are of no consequence.

The foregoing has been a description of the basic building blocks of the system. These are used to construct the larger scale of four, six, ten, and 16 counters. It was realized that the A card (shown in Figures 46 and 47) is the most complex because it is a decade with active feedback gating, and requires presetting. Since an A card layout had to be made in any event, the other counter cards, being simply an A card with small modifications or omissions, were automatically laid out. The additional complexity caused by unused printed track presented no problem because eight identical cards were photographically reproduced. The back of the cards (track side) are identical and is shown in Figure 48.

The A card is a high-speed decade counter consisting of four flip-flops, a NOR for active feedback gating, and an output NOR. The use of an output NOR is simply a practical matter of attaining the necessary fan-out ratio. It serves no logical function other than inversion, which is corrected using the one side of the last flip-flop to produce an output in the proper logical sense.

The decade counting scheme is accomplished by the circuit of Figure 46. Figure 46, the logic notation used is such that the barred side of the flip-flop is the ZERO side. The ON state is the ONE state, and the OFF state, the ZERO state. Suppose the counter is initially set on decimal zero. The count progresses in the normal binary manner to the fourth count, at which time the count corresponds to binary four. The state of binary four conditions

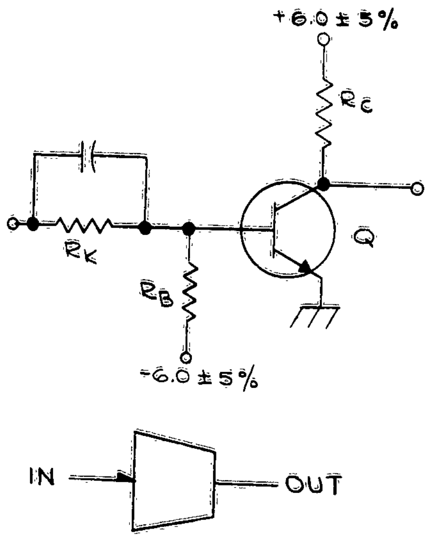


Figure 44. Inverter Amplifier

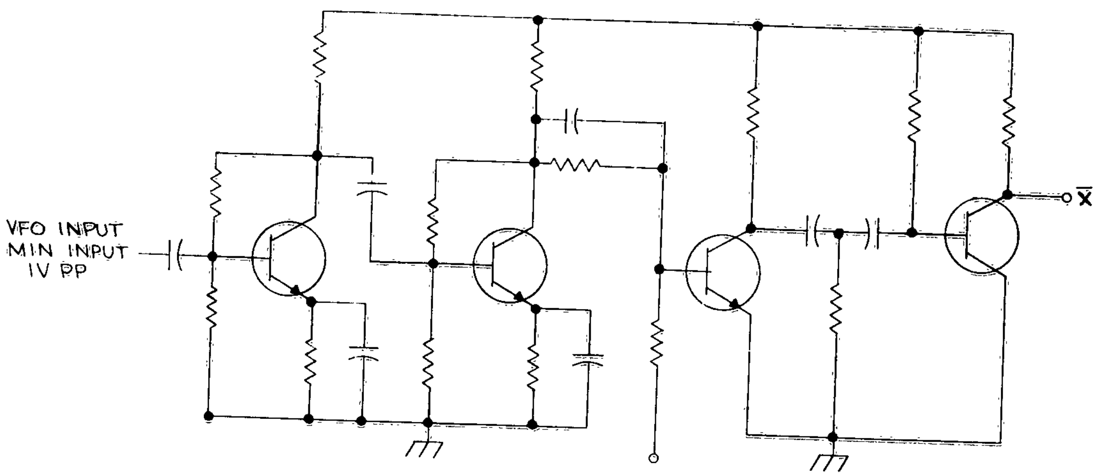


Figure 45. Broadband Amplifier and Pulse Former

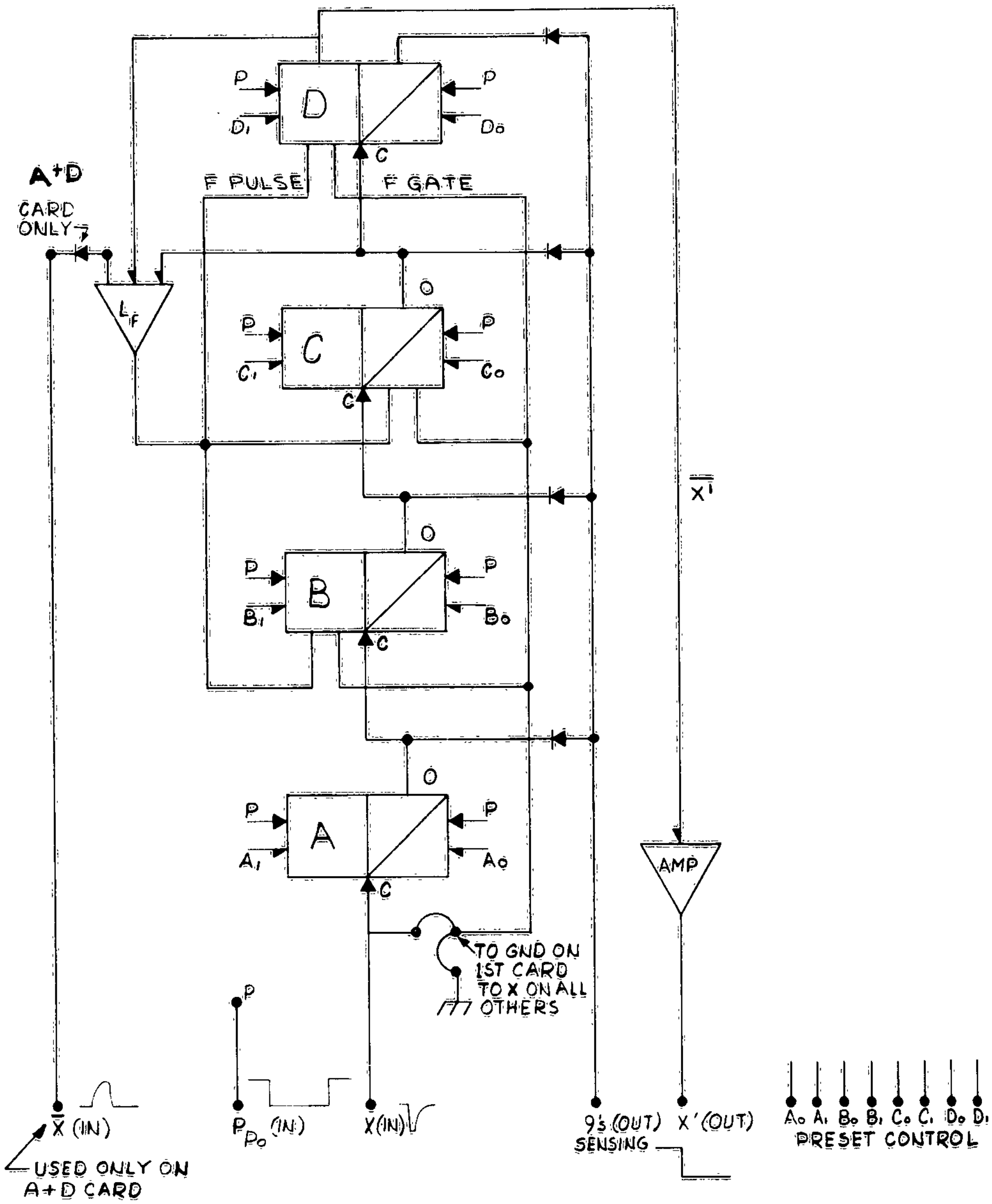


Figure 46. Block Diagram of Card A

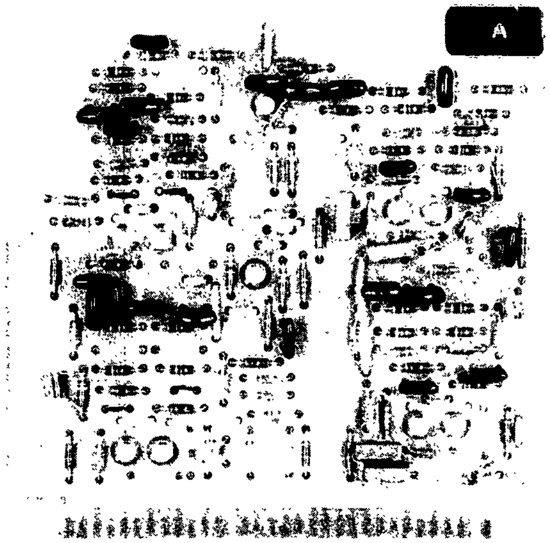


Figure 47. Component Side of Card A

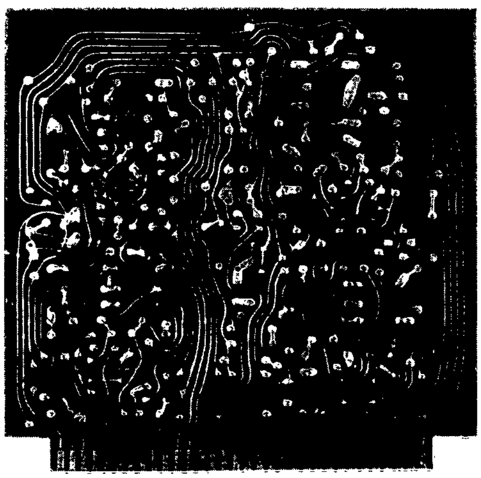


Figure 48. Track Side of Card A

the feedback NOR, LF, such that receipt of the fifth count causes binary eleven to occur. The count then proceeds normally to binary sixteen, or zero. The reason for this unorthodox method of counting is to advance the count and delete six counts from a scale-of-sixteen counter in such a manner that there are no feed-back ambiguities arising from carry propagation. This scheme does not require any increase in counter speed, as in some decade schemes. The state of four was chosen to condition the feed-back gating because this number is reached with a relatively short propagation delay. The counting scheme of stages A, B, C and D are as follows:

Decimal State	D	C	B	A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	1	0	1	1
6	1	1	0	0
7	1	1	0	1
8	1	1	1	0
9	1	1	1	1

The entire circuit of Figure 46 may be visualized as a true decimal counter which has ten distinct states, of which the transition from nine to zero produces the carry. It may be preset to any of the ten states. The state of nine is sensed to effect the count transfer.

Since passive R-C diode gates in the feedback circuits would require very low impedances and impose severe loads, it was decided to use active gating in the highest speed decade. Just after the pulse which causes to count of four, the feedback NOR is unblocked. The $\bar{X}$ pulse supplied to the feed-back NOR can then pass through as an $\bar{X}$ pulse and advance the count. After the count is advanced the NOR again is blocked because the stages controlling the NOR have changed state. This counter has preset control. Eight control wires leave the decade and are controlled by a frequency selector switch.

The B card shown in Figure 49 is similar to the A card. It is a decade with preset control. The feedback gating is passive. There is an output NOR. Passive gating does not present the previously mentioned problem due to the reduced speed of operation. Passive gating is desirable at lower speeds since the feedback pulse may then be derived from the output of the previous card.

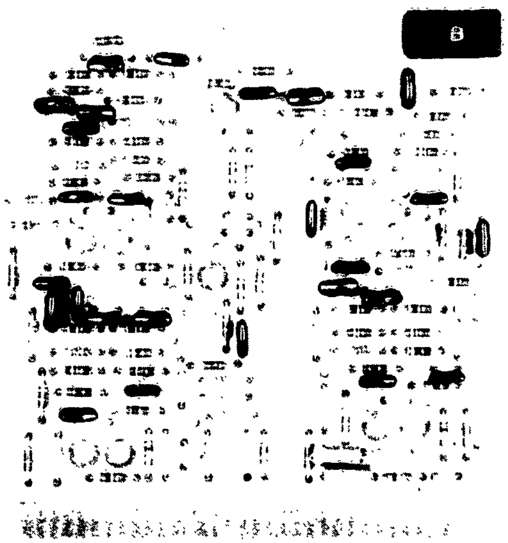


Figure 49. Component Side of Card B

It imposes no additional load on the $\bar{\bar{X}}$ source and requires one less diode. In the physical configuration R_{FC} and C_F are interchanged on the card. There are two identical B cards.

The C card, shown in Figure 50, is a scale of four counter with preset control. A NOR and an inverter/amplifier, also on this card, are part of the 9's sensing circuit. This is attained by the familiar means of using two flip-flops. Since it is not used to drive another unit, there is no output NOR. This counter is preset to either zero or one and counts to three. Therefore the presetting of the second flip-flop is always to the zero state. A single sided preset gate with its control resistor grounded is used on this flip-flop. Only two preset control wires are brought out to the hundreds switch.

The D card, shown in Figure 51, and E card, shown in Figure 52, are identical to the A card and B card respectively; except that there are no preset controls. All components associated with presetting are entirely omitted.

The F card, shown in Figure 53, is a scale of six counter consisting of three flip-flops and a feedback NOR. A NOR and an inverter/amplifier, also on this card, are part of the 9's sensing circuit. It drives no further counters, and requires no output NOR. Passive feedback gating is used. By replacing the usual first flip-flop with a jumper wire, and simply omitting the feedback gates to the flip-flop in the usual second place, a scale of six is attained.

Cards A through F all have 9's sensing diodes which sense the state of 9 on all decades (3 on the scale-of-four and 5 on the scale-of-six).

Card G, shown in Figure 54, is the scale-of-sixteen counter consisting of four flip-flops in the familiar connection. The purpose of this card is to precisely divide the reference frequency by sixteen to attain the same frequency as the desired VFO divided frequency. Also, on this card is a NOR which is used as a driver.

The H card, shown in Figure 55, or control card contains the broad-band amplifier and pulse forming circuits, the 9's sensing NOR's, the control flip-flop, the counter pulse gate NOR's, a 10 u second delay, and an amplifier for the preset pulse. Also on this card is a one microsecond single-shot which is used to generate the sample used in the phase detector.

When the cards were completed the work of interconnection was begun. It was at first found that the high speed circuits did not function as well as those built on break-off cards. It was found that greater capacitance to ground was causing a capacitor divider action. A slight increase in the input capacitors corrected the condition, as it theoretically should. This could not be observed directly due to the effect of the oscilloscope probe on the time constants.

After the individual cards were checked for proper operation sufficient connections were made to produce a scale of 4000 and a scale of 600 counters. Correct division at each card was verified by an oscilloscope.

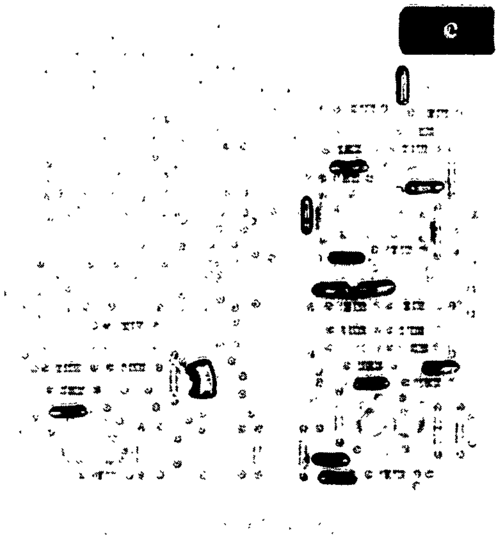


Figure 50. Component Side of Card C

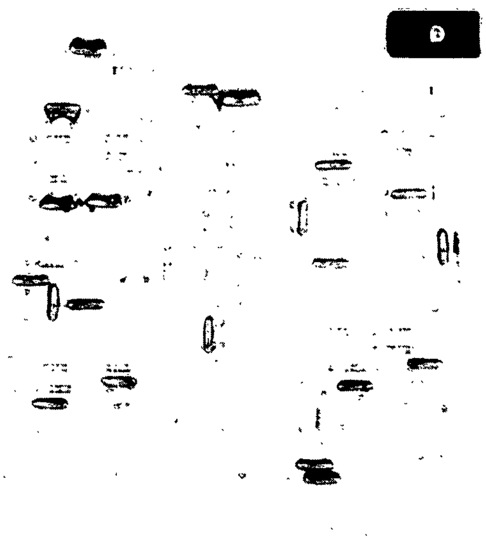


Figure 51. Component Side of Card D

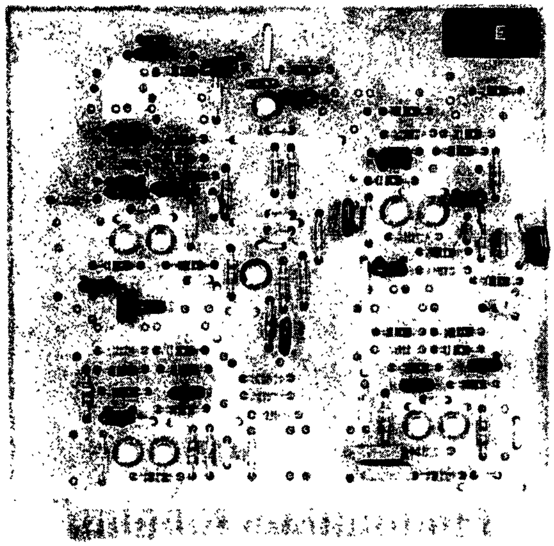


Figure 52. Component Side of Card E

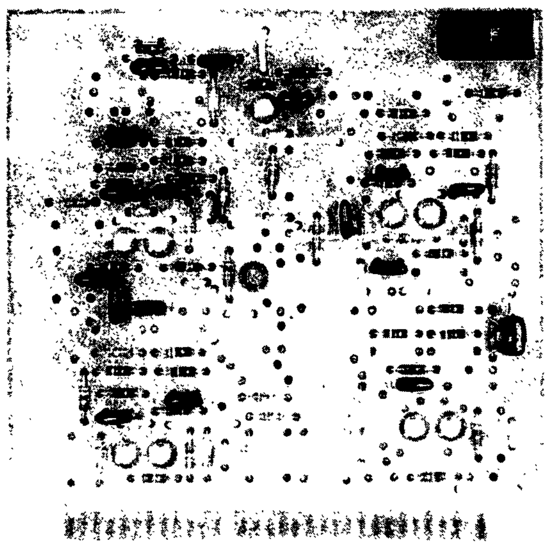


Figure 53. Component Side of Card F

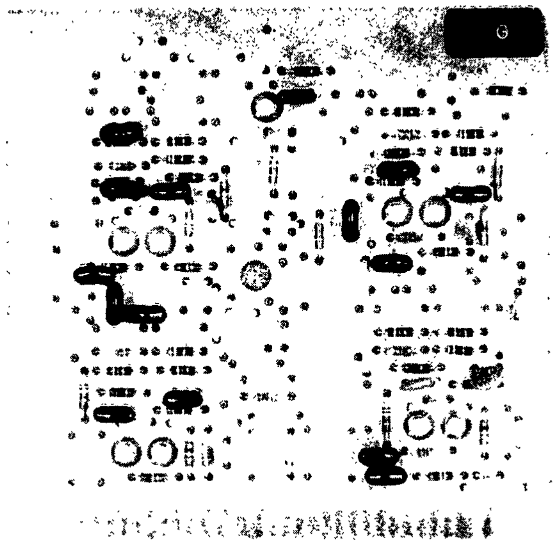


Figure 54. Component Side of Card G

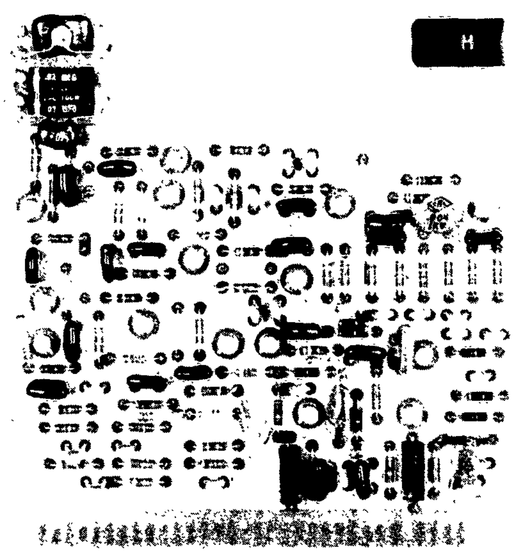


Figure 55. Component Side of Card H

The next operation was to connect the 9's sensing circuits and cause the counter to transfer between the scale of 4000 and the scale of 600 and vice-versa. It was here noted, by use of the external sync connected to the first card output, that the transition did not occur 9 counts after the output. Temporarily reducing the counter to a scale of 100 on each side remedied the trouble. Precise scale of 100 counting was verified as before, and by actual count on the oscilloscope. It was found that connecting the full number of diodes into the 9's sensing NOR was the cause. The apparent reason was that the first flip-flop of the A and D cards is the last to turn OFF and realease the NOR. The remaining diodes are back biased presenting a capacitance which momentarily presents a heavy load. The first flip-flop then failed to trigger until the second count. The nine sensing was divided so that the first decade goes directly to the 9's sensing NOR to prevent unnecessary delay. The remaining diodes go to a different NOR followed by an inverter; then to the 9's sensing NOR. The first decade of this group does not suffer this same trouble because the slower gates permit a longer pulse at the bases of these flip-flops, which can overcome the difficulty.

Proper operation, as a scale of 4000 and a scale of 600 counter, was then observed. The transition time was checked by connecting the external synchronous lead of the oscilloscope to the control flip-flop, and observing the counter gate outputs. Transition without missing or adding a count was positively verified by this means.

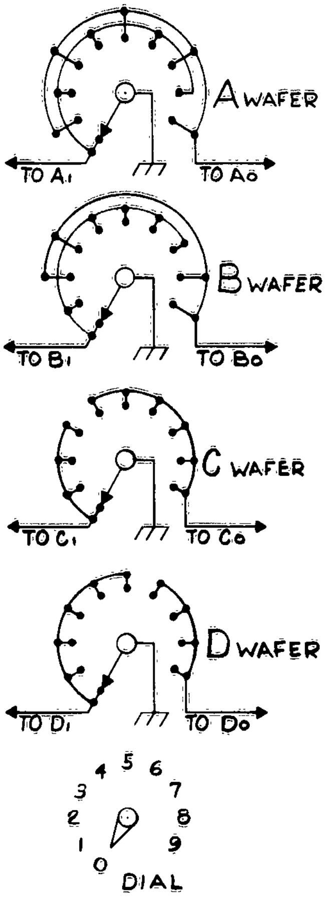
The device was then made to divide by any integer within the desired range by connecting the preset pulse line to all preset pulse inputs on the scale of 4000 side. The gates had previously been properly connected to the control switches. Operation was checked by synchronizing the oscilloscope with respect to the control flip-flop transition, such that the sweep started within a fixed delay of the instant the preset side began counting; and by using the "delayed sweep," feature of the oscilloscope to observe the last ten, or so, counts of the preset side counter gate. By this means, the last counts from the counter gate may be observed with improved resolution. Starting with the tenth megacycle dial on 9, one count should be deleted from the end of the train for each step the tenth knob is advanced counterclockwise. Similarly, by moving the probe to the output of the first decade, and appropriately changing the oscilloscope resolution, the output of the units megacycle control may be verified. Proper operation of the tens megacycle and hundreds megacycles dials may be checked by this technique, with the probe at the output of the second and third decade, respectively. To observe proper operation of the two most significant digits, it may be less complicated to use the "normal sweep" with the synchronization as before. This is in essence the same method because, in checking the most significant digits, adequate resolution can be obtained with the sweep delay of the oscilloscope set to zero, which is "normal sweep." Proper operation was observed in all positions, except when the tenths megacycle dial was set on "5". Under this condition the first decade should preset to the state of four. Since the state of four activates the feedback NOR, and active feedback is used; it was found that the preset pulse which passed through the preset gate did not end at the same instant on all stages of the decade. Thus the first stages released would then receive feedback, which would close the feedback NOR gate. The last stages released could not then receiver proper feedback. To remedy the situation, the preset controls were changed such that the dial position of 5 caused the counter to preset to a number not in the normal counting sequence. This number, designated as 4', was picked from those states which were deleted in making a scale of sixteen into a decade. It has the property that one count advances 4' to 5. Another property is that 4' does not activate the feedback NOR. When counting begins, the sequence is 4', 5, 6...2, 3, 4, 5.... This counting is as before and 4' is used only for presetting. No other number in the presetting sequence caused this problem. Since the following two decades do not use active pulse gating, the presence of the number 4 in the preset sequence does not present a problem. Either 4 or 4' may be desirable from the standpoint of consistency in wiring.

The wiring of the switches is a straight-forward matter of grounding the proper gate control wire. Figure 56 shows the proper connections. The preset gate control wires are labeled as A_1, B_1, C_1, D_1, A_0, B_0, C_0, D_0. The notation is such that grounding B_1, for example, conditions a proper preset gate to cause the preset pulse to force the B flip-flop of the decade to the ONE state. The wires with 0 subscripts are then used to condition the associated flip-flop to the zero state. To preset a decade to a given decimal number, one of the control wires from each flip-flop is grounded; or four out of eight control wires are grounded to preset the entire decade. It is necessary to control every flip-flop on both the ONE and ZERO side to prevent complementing action from causing an incorrect preset. Although this is a straight forward approach using readily available components, a smaller switch with fewer wafers might be made by using double wafers, special sectors, and etc.

Phase Detector:

The originally proposed phase detector was a simple device consisting of a NOR circuit that produced a 6250 cycle/sec rectangular waveform whose average value corresponded to the phase difference between the counter output and the reference frequency signal. This was added to the preset voltage, with DC restoring, and the result filtered to produce the error signal. This system produced a phase-lock and yielded the correct average frequency. The deficiency was that there was considerable 6250 cycle ripple in the control voltage, which in turn produced an FM deviation in the phase-locked oscillator.

Attempts to remedy this situation did not prove satisfactory. The obvious solution of providing additional low-pass filtering produced system instability, as was theoretically predicted. This method also imposed a severe limitation on the pull-in range. The frequency range over which the system can pull-in when



DIAL SETTING	Ao	A1	Bo	B1	Co	C1	Do	D1
0		G		G		G		G
1	G			G		G		G
2		G	G			G		G
3	G		G			G		G
4		G		G	G			G
5	G			G	G			G
6		G		G	G		G	
7	G			G	G		G	
8		G	G		G		G	
9	G		G		G		G	

G = GROUNDED

DECADE PRESET CONTROL SWITCH FOUR POLE (FOUR WAFER), TEN POSITION ROTARY SWITCH, ZERO DIAL POSITION SHOWN.
WHEN WIRED AS SHOWN, THE PROPER TRANSFORMATION HAS BEEN MADE TO MAKE THE DIAL READ THE CORRESPONDING DIGIT OF THE CARRIER FREQUENCY DIRECTLY.

Figure 56. Decode Preset Control Switch

out of lock is the true criterion of how accurately the preset voltage must be set. At best a compromise between pull-in range and ripple reduction had to be made. No practicable compromise was apparent.

At this point the general design philosophy was changed. Instead of attempting to use a filtered signal to correct a continuously controlled servo-mechanism, the device that was made was a sampled servo-mechanism. A phase-detector was needed which would hold the previous control voltage until the next counter cycle. If there were an error, it would be recognized and the correction process started immediately by causing the control voltage to step to a closer approximation of the correct value. If there were no error, there would be no change in control voltage. Thus, ripple is a function of diode leakage and stray signal pick up and not inherent to the system. In actual operation the control voltage response to on step displacement follows a converging series of steps which rapidly approach the correct value. In steady-state operation, the steps become imperceptably small. It was experimentally verified by examining the control voltage on a high gain oscilloscope that such a phase detector with a plus or minus 8.5 volt pull-in range could produce a control voltage with ripple in the millivolt range. At this point the use of shielding and stray coupling effects became an important consideration in further ripple and spurious pulse type deviations. Building the phase-detector on a shielded plug-in board using well filtered supply voltages produced an acceptable signal.

The phase-detector is built on a plug-in card (J) similar to the other digital equipment in the receiver. This is a double-sided card with the component-side (Figure 57) plating used as a shield. Figure 58 shows the track-side. There are ten transistors on this card and a total of approximately 70 components.

In Figure 59 the reference signal is a 6250 cycle/sec. square wave from the 16 divider card. The single-shot on this card is of conventional design. It produces a reset pulse to drive the sawtooth generator. The sawtooth generator is a modified Miller type sweep circuit with a diode network in the feedback path. This enables the device to sweep normally in the absence of a control pulse. The control pulse causes the sweep to quickly return to the starting position. At this time the diodes allow rapid recovery of the feedback capacitor. The sawtooth signal drives the complementary emitter followers to produce a very low impedance saw-tooth voltage necessary for the sampler. The output of the counter is used to produce a pulse which is amplified and used to gate the sampler. The sampler is a bilateral gate which momentarily connects the sawtooth voltage to the capacitor analogue memory. The sampler consists of a small torroidal pulse transformer, two capacitors, two resistors, and two low leakage diodes. Within the sampler, the signal is split into two pulses which are later recombined. Before combining the pulses pass through capacitors which permits the preset voltage to be added to the pulses through a return resistor. After the sampling pulse occurs, the diodes block the memory capacitor discharge path. The control

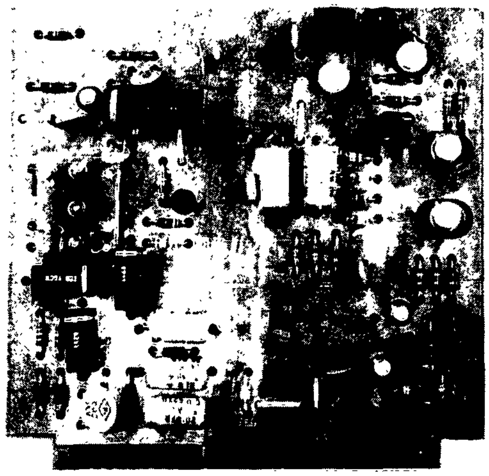


Figure 57. Component Side of Card J

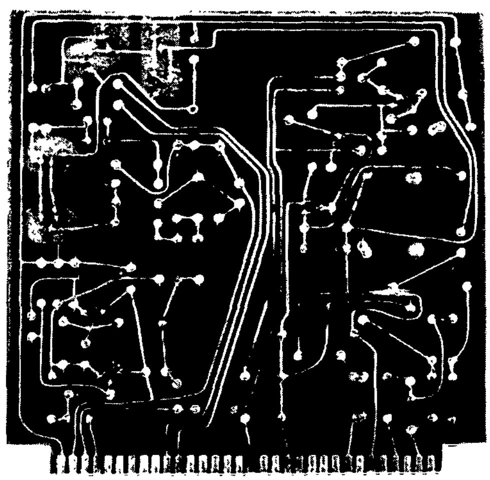


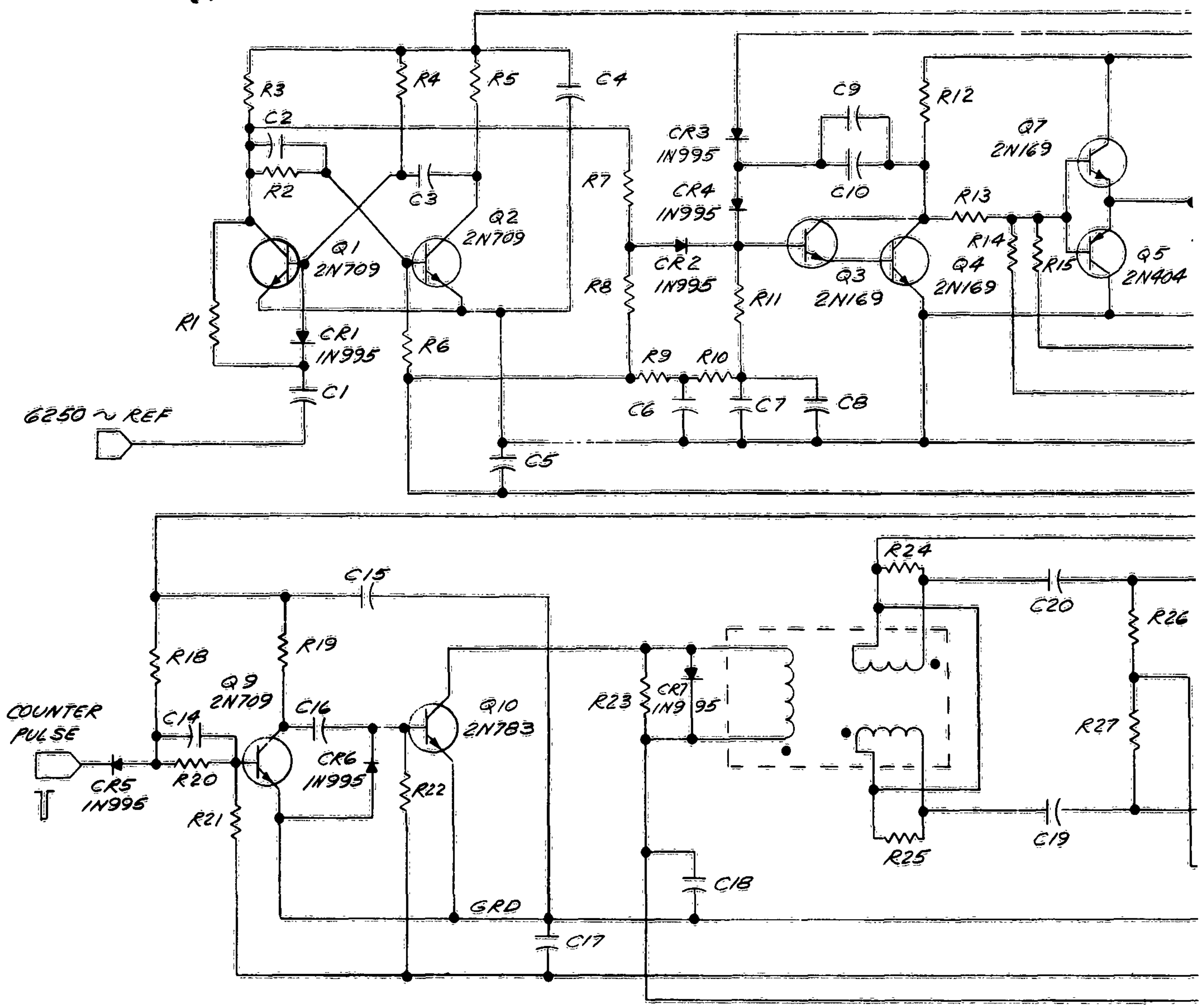
Figure 58. Track Side of Card J

voltage then holds essentially constant until the next sample. The polarities of the sawtooth are chosen such that if the oscillator frequency is low, sampling will occur later and at a higher point on the sawtooth than the previous sample. This raises the frequency. Similarly, the control operates in the opposite direction to lower the frequency. Since this is a null-seeking device, the inherent accuracy is not affected by slight variations in the phase detector components; but rather by the reference frequency accuracy. The open-loop gain of the servo may be computed, knowing the reference frequency, the voltage-frequency sensitivity of the VFO and the sawtooth slope. It can be shown that:

$$fc = fr \left[1-(1-K)^n\right] .$$

Where fc is the controlled frequency; fr, the reference frequency; K, the open loop gain; and n the number of connections made. Examination shows the function to be convergent for any falue of K between zero and two, with exact connection in one step with K exactly equal to one. For K near 1, convergence is rapid. Thus, in a practical circuit, considerable tolerance in K is permissible. For example, if K lies between 0.5 and 1.5 the error is reduced by one half after each connection, which is every 160 μ seconds in the UHF receiver synthesizer which was built.

11


R3
R4
R5
C4
C2
R2
C3
Q2
2N709
Q1
2N709
R1
CR1
1N995
R6
C1
6250 ~ REF
C5
R7
CR3
1N995
CR4
1N995
CR2
1N995
R8
R9
R10
R11
C6
C7
C8
C9
C10
R12
Q7
2N169
R13
R14
R15
Q3
2N169
Q4
2N169
Q5
2N404
C15
R18
R19
Q9
2N709
C14
C16
Q10
2N783
COUNTER
PULSE
CR5
1N995
R20
CR6
1N995
R21
R22
GRD
C17
R23
CR7
1N995
C18
R24
R25
C20
C19
R26
R27

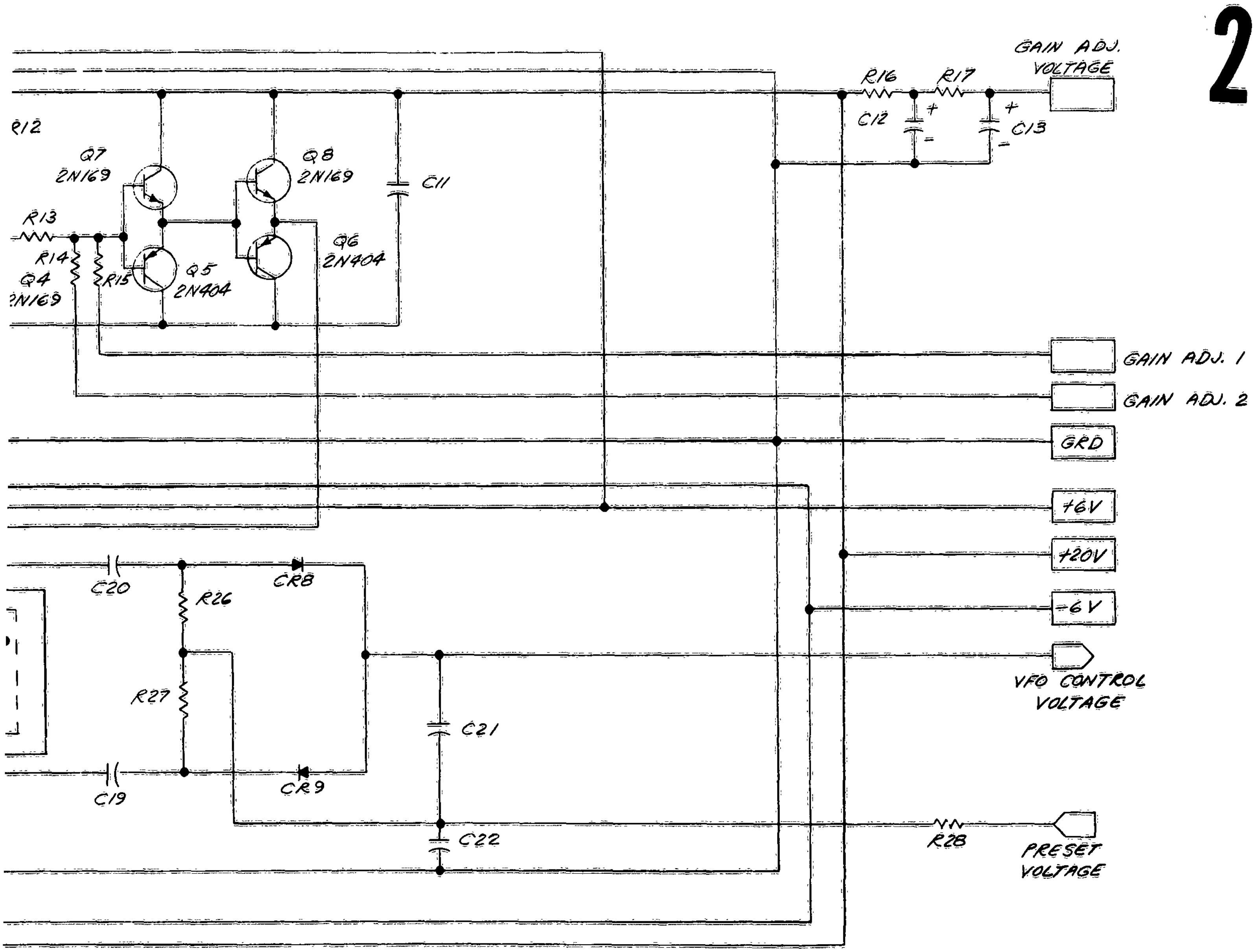


Figure 59. Electronic Tuning Sampled Phased Detector

DISTRIBUTION LIST
ASD-TDR-62-1033

Number of Copies	Activity
2	ASD (ASRNCS-3) Wright-Patterson AFB, Ohio
1	ASD (ASAPR) Wright-Patterson AFB, Ohio
3	ASD (ASAPT) Wright-Patterson AFB, Ohio
4 or more	ASTIA (TIPDR) Arlington Hall Sta Arlington 12 Va
1	AFCRL (CRRS/Robert M. Alexander) L G Hanscom Fld Bedford Mass
1	RADC (RAUA/Albert Feiner) Griffiss AFB NY
1	RADC (RAUED/David A. Bone) Griffiss AFB NY
1	SSD (SSTRG/Capt John F. Tiernan) AF Unit Post Office Los Angeles 45, California
1	Commanding Officer US Army Signal Research & Development Laboratories Attn: Technical Document Center Ft. Monmouth, New Jersey
1	Chief of Naval Research Dept. of the Navy Washington 25, D.C.
1	Federal Aviation Agency Bureau of Research & Development Attn: Record Officer Washington 25, D.C.

Number of Copies	Activity
1	Director National Security Agency Attn: CREF (Room 2C087) Ft. George G. Meade, Maryland
1	Director Langley Research Center National Aeronautics & Space Administration Attn: Librarian Langley Field, Virginia
1	Chief, Technical Library Office of Asst. Sec of Defense (R&D) Room 3E 1065, The Pentagon Washington 25, D.C.
1	USAFA US Air Force Academy Colorado
1	AFSC (SCRC) Andrews AFB Washington 25, D.C.
1	Air University Attn: Library Maxwell AFB, Alabama
1	Dept. of the Army Attn: Library Washington 25, D.C.
1	Director, Communication Dept. Telecommunications Division US Army Signal Engineering Lab. Ft. Monmouth, New Jersey

Aeronautical Systems Division, Dir/Avionics, Electromagnetic Warfare & Communications Lab, Wright-Patterson AFB, Ohio
Rpt Nr ASD-TDR-1033, THE AUTOMATIC REMOTE TUNING SYSTEM FOR GROUND-AIR UHF COMMUNICATIONS. Final Technical Report, January 1963, 100 pages including illustrations.
Unclassified Report

The objective of this contract was to develop two control systems. One, an Automatic Remote Tuning System for ground-air UHF communications, and the other system, a UHF Solid State Tuning Device utilizing all solid state components.

The Automatic Remote Tuning System is a system which tunes an airborne AN/ARC-34 UHF communications transceiver from the ground through the

1. Communications Systems
2. Electronic Circuits
3. Tuning Circuits
4. Tuning Devices

I. AFSC Project 4335, Task 4335D8
II. Contract No. AF33(616)7311
III. The Bendix Corporation, Bendix Radio Division, Baltimore 4, Maryland
IV. Author's name W. D. Phillips
V. 471-938-490
VI. Not available fr OTS
VII. Not aval fr ASTIA

Aeronautical Systems Division, Dir/Avionics, Electromagnetic Warfare & Communications Lab, Wright-Patterson AFB, Ohio
Rpt Nr ASD-TDR-1033, THE AUTOMATIC REMOTE TUNING SYSTEM FOR GROUND-AIR UHF COMMUNICATIONS. Final Technical Report, January 1963, 100 pages including illustrations.
Unclassified Report

The objective of this contract was to develop two control systems. One, an Automatic Remote Tuning System for ground-air UHF communications, and the other system, a UHF Solid State Tuning Device utilizing all solid state components.

The Automatic Remote Tuning System is a system which tunes an airborne AN/ARC-34 UHF communications transceiver from the ground through the

1. Communications Systems
2. Electronic Circuits
3. Tuning Circuits
4. Tuning Devices

I. AFSC Project 4335, Task 4335D8
II. Contract No. AF33(616)7311
III. The Bendix Corporation, Bendix Radio Division, Baltimore 4, Maryland
IV. Author's name W. D. Phillips
V. 471-938-490
VI. Not available fr OTS
VII. Not aval fr ASTIA

Aeronautical Systems Division, Dir/Avionics, Electromagnetic Warfare & Communications Lab, Wright-Patterson AFB, Ohio
Rpt Nr ASD-TDR-1033, THE AUTOMATIC REMOTE TUNING SYSTEM FOR GROUND-AIR UHF COMMUNICATIONS. Final Technical Report, January 1963, 100 pages including illustrations.
Unclassified Report

The objective of this contract was to develop two control systems. One, an Automatic Remote Tuning System for ground-air UHF communications, and the other system, a UHF Solid State Tuning Device utilizing all solid state components.

The Automatic Remote Tuning System is a system which tunes an airborne AN/ARC-34 UHF communications transceiver from the ground through the

1. Communications Systems
2. Electronic Circuits
3. Tuning Circuits
4. Tuning Devices

I. AFSC Project 4335, Task 4335D8
II. Contract No. AF33(616)7311
III. The Bendix Corporation, Bendix Radio Division, Baltimore 4, Maryland
IV. Author's name W. D. Phillips
V. 471-938-490
VI. Not available fr OTS
VII. Not aval fr ASTIA

Aeronautical Systems Division, Dir/Avionics, Electromagnetic Warfare & Communications Lab, Wright-Patterson AFB, Ohio
Rpt Nr ASD-TDR-1033, THE AUTOMATIC REMOTE TUNING SYSTEM FOR GROUND-AIR UHF COMMUNICATIONS. Final Technical Report, January 1963, 100 pages including illustrations.
Unclassified Report

The objective of this contract was to develop two control systems. One, an Automatic Remote Tuning System for ground-air UHF communications, and the other system, a UHF Solid State Tuning Device utilizing all solid state components.

The Automatic Remote Tuning System is a system which tunes an airborne AN/ARC-34 UHF communications transceiver from the ground through the

1. Communications Systems
2. Electronic Circuits
3. Tuning Circuits
4. Tuning Devices

I. AFSC Project 4335, Task 4335D8
II. Contract No. AF33(616)7311
III. The Bendix Corporation, Bendix Radio Division, Baltimore 4, Maryland
IV. Author's name W. D. Phillips
V. 471-938-490
VI. Not available fr OTS
VII. Not aval fr ASTIA

selective calling AN/URA-22 (Discom) system. The equipment is completely of solid state construction.

The UHF Solid State Tuning Device is a 1750 channel UHF receiver which is tuned by use of varactor diodes. There are no moving parts in the receiver. The frequency synthesizer is also unique in that all frequencies are obtained from a single crystal oscillator and are phase locked to this stable source.

selective calling AN/URA-22 (Discom) system. The equipment is completely of solid state construction.

The UHF Solid State Tuning Device is a 1750 channel UHF receiver which is tuned by use of varactor diodes. There are no moving parts in the receiver. The frequency synthesizer is also unique in that all frequencies are obtained from a single crystal oscillator and are phase locked to this stable source.

selective calling AN/URA-22 (Discom) system. The equipment is completely of solid state construction.

The UHF Solid State Tuning Device is a 1750 channel UHF receiver which is tuned by use of varactor diodes. There are no moving parts in the receiver. The frequency synthesizer is also unique in that all frequencies are obtained from a single crystal oscillator and are phase locked to this stable source.

selective calling AN/URA-22 (Discom) system. The equipment is completely of solid state construction.

The UHF Solid State Tuning Device is a 1750 channel UHF receiver which is tuned by use of varactor diodes. There are no moving parts in the receiver. The frequency synthesizer is also unique in that all frequencies are obtained from a single crystal oscillator and are phase locked to this stable source.

Aeronautical Systems Division, Dir/Avionics, Electromagnetic Warfare & Communications Lab, Wright-Patterson AFB, Ohio
Rpt Nr ASD-TDR-1033, THE AUTOMATIC REMOTE TUNING SYSTEM FOR GROUND-AIR UHF COMMUNICATIONS. Final Technical Report, January 1963, 100 pages including illustrations.
Unclassified Report

The objective of this contract was to develop two control systems. One, an Automatic Remote Tuning System for ground-air UHF communications, and the other system, a UHF Solid State Tuning Device utilizing all solid state components.

The Automatic Remote Tuning System is a system which tunes an airborne AN/ARC-34 UHF communications transceiver from the ground through the

1. Communications Systems
2. Electronic Circuits
3. Tuning Circuits
4. Tuning Devices

I. AFSC Project 4335, Task 4335D8
II. Contract No. AF33(616)7311
III. The Bendix Corporation, Bendix Radio Division, Baltimore 4, Maryland
IV. Author's name W. D. Phillips
V. 471-938-490
VI. Not available fr OTS
VII. Not aval fr ASTIA

Aeronautical Systems Division, Dir/Avionics, Electromagnetic Warfare & Communications Lab, Wright-Patterson AFB, Ohio
Rpt Nr ASD-TDR-1033, THE AUTOMATIC REMOTE TUNING SYSTEM FOR GROUND-AIR UHF COMMUNICATIONS. Final Technical Report, January 1963, 100 pages including illustrations.
Unclassified Report

The objective of this contract was to develop two control systems. One, an Automatic Remote Tuning System for ground-air UHF communications, and the other system, a UHF Solid State Tuning Device utilizing all solid state components.

The Automatic Remote Tuning System is a system which tunes an airborne AN/ARC-34 UHF communications transceiver from the ground through the

1. Communications Systems
2. Electronic Circuits
3. Tuning Circuits
4. Tuning Devices

I. AFSC Project 4335, Task 4335D8
II. Contract No. AF33(616)7311
III. The Bendix Corporation, Bendix Radio Division, Baltimore 4, Maryland
IV. Author's name W. D. Phillips
V. 471-938-490
VI. Not available fr OTS
VII. Not aval fr ASTIA

Aeronautical Systems Division, Dir/Avionics, Electromagnetic Warfare & Communications Lab, Wright-Patterson AFB, Ohio
Rpt Nr ASD-TDR-1033, THE AUTOMATIC REMOTE TUNING SYSTEM FOR GROUND-AIR UHF COMMUNICATIONS. Final Technical Report, January 1963, 100 pages including illustrations.
Unclassified Report

The objective of this contract was to develop two control systems. One, an Automatic Remote Tuning System for ground-air UHF communications, and the other system, a UHF Solid State Tuning Device utilizing all solid state components.

The Automatic Remote Tuning System is a system which tunes an airborne AN/ARC-34 UHF communications transceiver from the ground through the

1. Communications Systems
2. Electronic Circuits
3. Tuning Circuits
4. Tuning Devices

I. AFSC Project 4335, Task 4335D8
II. Contract No. AF33(616)7311
III. The Bendix Corporation, Bendix Radio Division, Baltimore 4, Maryland
IV. Author's name W. D. Phillips
V. 471-938-490
VI. Not available fr OTS
VII. Not aval fr ASTIA

Aeronautical Systems Division, Dir/Avionics, Electromagnetic Warfare & Communications Lab, Wright-Patterson AFB, Ohio
Rpt Nr ASD-TDR-1033, THE AUTOMATIC REMOTE TUNING SYSTEM FOR GROUND-AIR UHF COMMUNICATIONS. Final Technical Report, January 1963, 100 pages including illustrations.
Unclassified Report

The objective of this contract was to develop two control systems. One, an Automatic Remote Tuning System for ground-air UHF communications, and the other system, a UHF Solid State Tuning Device utilizing all solid state components.

The Automatic Remote Tuning System is a system which tunes an airborne AN/ARC-34 UHF communications transceiver from the ground through the

1. Communications Systems
2. Electronic Circuits
3. Tuning Circuits
4. Tuning Devices

I. AFSC Project 4335, Task 4335D8
II. Contract No. AF33(616)7311
III. The Bendix Corporation, Bendix Radio Division, Baltimore 4, Maryland
IV. Author's name W. D. Phillips
V. 471-938-490
VI. Not available fr OTS
VII. Not aval fr ASTIA

selective calling AN/URA-22 (Discom) system. The equipment is completely of solid state construction.

The UHF Solid State Tuning Device is a 1750 channel UHF receiver which is tuned by use of varactor diodes. There are no moving parts in the receiver. The frequency synthesizer is also unique in that all frequencies are obtained from a single crystal oscillator and are phase locked to this stable source.

selective calling AN/URA-22 (Discom) system. The equipment is completely of solid state construction.

The UHF Solid State Tuning Device is a 1750 channel UHF receiver which is tuned by use of varactor diodes. There are no moving parts in the receiver. The frequency synthesizer is also unique in that all frequencies are obtained from a single crystal oscillator and are phase locked to this stable source.

selective calling AN/URA-22 (Discom) system. The equipment is completely of solid state construction.

The UHF Solid State Tuning Device is a 1750 channel UHF receiver which is tuned by use of varactor diodes. There are no moving parts in the receiver. The frequency synthesizer is also unique in that all frequencies are obtained from a single crystal oscillator and are phase locked to this stable source.

selective calling AN/URA-22 (Discom) system. The equipment is completely of solid state construction.

The UHF Solid State Tuning Device is a 1750 channel UHF receiver which is tuned by use of varactor diodes. There are no moving parts in the receiver. The frequency synthesizer is also unique in that all frequencies are obtained from a single crystal oscillator and are phase locked to this stable source.